Supplementary Information

Sabbir A. Khan,[*,†,‡] Charalampos Lampadaris,[†,‡] Ajuan Cui,[†,‡] Lukas Stampfer,[‡] Yu Liu,[†,‡] S. J. Pauka,[¶] Martin E. Cachaza,[†,‡] Elisabetta M. Fiordaliso,[§] Jung-Hyun Kang,[†,‡] Svetlana Korneychuk,[‖] Timo Mutas,[‡] Joachim E. Sestoft,[‡] Filip Krizek,[‡] Rawa Tanta,[†,‡] M. C. Cassidy,[¶] Thomas S. Jespersen,[‡] and Peter Krogstrup[*,†,‡]

†*Microsoft Quantum Materials Lab Copenhagen, 2800 Lyngby, Denmark*

‡*Center for Quantum Devices, Niels Bohr Institute, University of Copenhagen, 2100 Copenhagen, Denmark*

¶*Microsoft Quantum Sydney, The University of Sydney, Sydney, NSW 2006, Australia*

§*DTU Nanolab, Technical University of Denmark, 2800 Kgs. Lyngby, Denmark*

‖*QuTech and Kavli Institute of Nanoscience, Delft University of Technology, 2600 GA Delft, The Netherlands*

E-mail: sabbir.khan@nbi.ku.dk; krogstrup@nbi.dk

S1. Experimental Details

Substrate Fabrication for NW Growth. InAs (100) undoped (Un) single side polished (SSP) 500 μm thick 2-inch wafer (from WaferTech. Ltd.) is used to start the substrate fabrication for hybrid NW growths. Substrate preparation is discussed below:

Step 1: For exposure, we use electron sensitive co-polymer resist EL9 and spin with 4000 RPM speed (thickness 320 nm) for 45 sec. Next, hotplate baking of the resist is performed at 185°C for 2 min in order to get rid of the solvent and improve the adhesion with the substrate.

Lines for the trenches are exposed with electron beam lithography (EBL) Elionix ELS 700, 100 KeV system using 500 pA current, 40 μm aperture, write field size of 60000 dots / 300 μm and dose time of 300 μs/dot. For development we dip the wafer into 1:3 MIBK: IPA for 45 sec and IPA for 30 sec followed by oxygen plasma treatment for 2 min. **Step 2**: Wet etching to create (111) B faceted trenches. We etch the exposed lines to create V-shaped trenches with an angle of 54.7° using following recipe: i) Mix H_2SO_4 (1 ml): H_2O_2 (8 ml): H_2O (80 ml) and blend for 5 min with magnetic stirrer. ii) take 4 ml of above mixture, mix with 400 ml of H_2O, and blend for 5 min with magnetic stirrer. The wafer is dipped in the solution for 30 min (for $\sim$ 1 μm etching) or 60 min (for $\sim$ 2 μm etching), followed by a cleaning procedure. The steps for cleaning are: i) Acetone for 4 min, ii) sonication for 2 min with 80 Hz frequency and 30 W power, iii) acetone for 10 sec, iv) IPA for 10 sec and finally clean with milli-q water for 30 sec. **Step 3**: Dots exposure for Au particles. Two layers of resist are needed in order to coat homogeneously on the trenches. First, EL6 spinning with 4000 RPM speed (150 nm) for 45 sec followed by baking in a hotplate 1 min at 185°C, second, A2 spinning with 4000 RPM speed (60 nm) for 45 sec and similar hotplate baking 1 min at 185°C. Same EBL system and conditions (Step 2) are used for dots exposure varying the dose time from 100 to 300 μs/dot. For post-exposure dots development, we dip the wafer into 1:3 MIBK: IPA for 45 sec, IPA for 30 sec, followed by examination with the optical microscopy to confirm that the dots are properly aligned with the trenches. **Step 4**: Au film deposition on the wafer. Depending on the NW diameter, 12-15 nm Au layer is deposited at the rate of 1 Å/s on the wafer using e-beam evaporator (ATC 1800-HY AJA International System). If there is a time delay between resist development and Au deposition, it is crucial to remove the native oxide before Au deposition through Hydrofluoric acid (HF) dipping or *in-situ* Ar milling in metal evaporation chamber. However, this is not needed if the Au deposition is immediately after the development. For lift-off, Au consisted wafer is immersed onto the Acetone and kept for 10 min until the Au started lifting-off and then a pipette is used to blow out the Au film. Later, the acetone dipped sample is placed into 50°C heated bath for

1 hour and blown out with pipette again in order to completely remove the Au layer leaving only Au disks on resist-free area. Post-lift-off cleaning procedure of the wafer is similar to step 2. Finally, the ready-to-grow 2-inch InAs (100) wafer is cleaved into four quarters to make it adjustable with the MBE growth holder and plasma ashed for 2 min (similar to step 1) to make sure no organic particle is left on the quarter. Now each quarter is ready for NW growth.

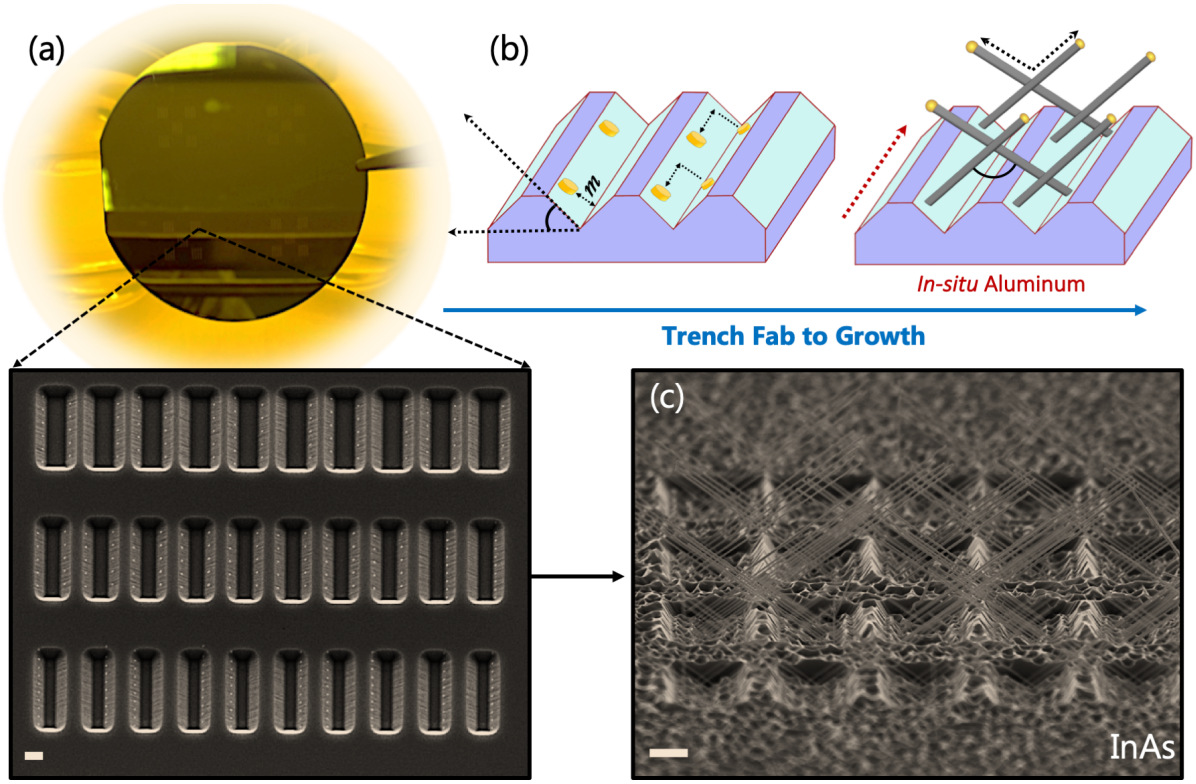

Figure 1: **Substrate fabrication and molecular beam epitaxy of hybrid nanowires a**, An image of 2-inch wafer with lithography-defined patterns. Zoomed-in SEM image of the (111) B faceted trenches with deposited Au disks (scale bar is 1 μm). **b**, Schematic of the fabricated substrate and NW growth scheme. Exact angle of the etched trenches are 54.7°C. An offset (m) from the bottom of the trenches is maintained in order to avoid competition between bulk growth and NW growth in the trenches. Regarding the position of the Au, if it is close to the lower edge of the trench, the wire may not be able to grow before it gets covered by planner growth. If the catalyst is too close to the upper edge, it migrates to the (100) facet while annealing. Hence, perfectly aligned lithography to place the Au seeds in the middle of the sidewall is crucial. Red arrow is the SU deposition direction along the trenches. **c**, An example of InAs NWs growth from the trench substrate.

Hybrid NWs Synthesis using MBE. Semiconductor hybrid NWs are grown using Veeco Gen II MBE system. Prior to loading in the MBE chamber, the fabricated wafer (1/4 of 2-inch wafer) is dipped into diluted HF for 10 sec, followed by 20 sec of rinsing with the milli-q water in order to make sure substrate and Au disk are clean for loading. Initially the sample is baked at 200°C for 2 hours in entry/exit (EE) chamber of the MBE system which confirms vaporization of remaining water molecule from the system and make sure the sample is ready to transfer in high vacuum buffer/ transfer chamber. In the buffer chamber the sample is degassed for 1 hour at 250°C where the holder is directly in contact with thermal heating to confirm additional cleaning before transferring into the growth chamber. In the growth chamber, growth substrates are annealed for 2 min at 590°C. It takes 6 min (with linear increment) to reach 590°C from base the temperature 200°C. All the intended effusion cells are usually heated up and flux is stabilised before the growth. InAs NWs on the trench are grown with arsenic over-pressure where As_4 is being used maintaining bulk temperature at 345°C and cracker temperature 400°C. Right after annealing the substrate is cooled down to growth temperature within 5 min (linear cooling) and stabilised for 3 min followed by In shutter opening. Right after the NW growth, substrate is cool down to 150°C and all the sources are set back to the base temperature. InSb NWs are grown with initial InAs NW stem where the growth procedure of stem is exactly same as described above. Maintaining same substrate temperature, As shutter is closed and Sb shutter is open leading to InSb NW growth continues from the InAs stem. Finally, $InAs_{0.3}Sb_{0.7}$ NWs are also grown with InAs stem assistance similar to InSb NWs growth where Sb shutter is opened and we tune the As flux for different compositions. *In-situ* Al deposition is performed in the MBE growth chamber by cooling down the substrate holder to ~ -36°C over the period of 8-10 hours right after the growth. When the desired temperature is reached the substrate is aligned to the intended deposition angle for Al growth on the wires and shadowing. Prior to the deposition, Al cell is heated 1140°C and flux is stabilised. 15 min of O_2 venting is performed while taking out NW from MBE chamber in order to form AlO_X to avoid dewetting. Sn and

Pb on the NWs are grown in metal deposition chamber (MDC) which is directly connected to MBE maintaining high vacuum. Growth details of Sn and Pb on NWs will be discussed in the follow-up articles [1, 2].

Structural Characterization of the Hybrid NWs. The morphology along with length and diameter of the grown NWs are examined with SEM (JEOL JSM-7800F). AFM (Bruker Dimension Icon) is also used to characterize surface morphology of the junctions, analyze broadening and also to determine the thickness of SU. The atomic crystal structures of the NWs are characterized by TEM, high resolution (HR-) TEM (Tecnai T20 G2, HT 200 kV, Gatan 894 Pre GIF CCD 2K USC 1000 camera). The structural properties, including lattice constant and atomic configuration, are analyzed using CrystalMaker for Windows (Ver. 9.2.7, CrystalMaker Software Ltd.). For STEM-Tomography: NWs are transferred from the growth substrate onto a TEM grid with a lacey carbon membrane using micromanipulator. The grid is mounted on a Gatan tomography TEM holder, allowing tilting of samples from -70 to 70 degrees. A Thermo Fisher Scientific S/TEM Talos F200X microscope is used to acquire HAADF-STEM images at 200 kV, at steps of 1 degree. The Thermo Fisher Scientific Inspect 3D software is used for image alignment and reconstruction. 3D visualization is performed by the Thermo Fisher Scientific Avizo software.

NW Device Fabrication. Device fabrication starts with transferring wires onto the pre-fabricated back-gated device chip using micromanipulator. 2 min of plasma ashing is performed prior to transferring NWs on the chip. Hybrid NW devices with SE-SU junctions are fabricated as following: for InAs devices, 1) spin electron sensitive PMMA resist (A4) on the chip with 4000 RMP speed (320 nm) for 45 sec and bake at 180°C for 2 min. 2) E-beam lithography for source and drain electrode using 500 pA current and aperture 40 μm. 3) For development, 1:3 MIBK: IPA for 45 sec, rinse in IPA for 30 sec and later oxygen plasma treatment for 2 min. 4) To remove the oxidised nanowire surface and better contact plasma enhanced RF milling is done for 4 min. with 20 W before depositing e-beam evaporated Ti and Au (5 nm and 250 nm) in rate of 1.5 Å/s. 5) Lift-off is done using acetone for 20

min and blow out with pipette. 6) Cleaning procedure is done by rinsing with acetone, dipping on IPA for 10 sec followed by 2 min oxygen plasma. 7) Finally, the chip is sealed on the daughter board and copper wire bonding is done with pre-patterned Au plate of the chip. For $InAs_{0.3}Sb_{0.7}$ devices, we follow the similar procure as mentioned above. The only change is resist baking at 115°C for 2 min. For InSb devices, no hotplate baking is performed after resist spinning as InSb/Al is subjected to high temperature , instead pump out in the microwave in performed for 2 hours.

PPMS measurements. For electrical measurement, physical property measurement system (PPMS, Quantum Design Inc.) is used with $\sim$ 2 K and 9 T magnetic field. The device chip with daughter board is mounted in the motherboard and loaded in the PPMS system. Then the PPMS system is pumped maintaining $\sim$ 4 mTorr followed by around 10 hours of degassing at 350 K. For InSb/Al and $InAs_{0.3}Sb_{0.7}$/Al devices the degassing process in not performed due to the risk of damaging the interface with high temperature. PPMS is then cooled down to 10 K and supply evaporated liquid helium (H_4) in the chamber to further cool down to $\sim$ 2 K.

20 mK measurements. The devices for the superconducting measurements are fabricated on degenerately doped Si substrates with 200 nm of thermal oxide substrates. The contact areas are patterned using standard electron beam lithography. The contact materials are Ti/Au (5/195 nm) after an in-situ Argon milling process. The measurements are performed in a cryo-free dilution refrigerator at a base temperature of 20 mK. Critical current measurements are performed using standard Lock-In and DC techniques with the use of a 50 kΩ shunt resistor. The clearly identifiable supercurrent shows a residual resistance. This is attributed contact resistance and subtracted from the dataset. The nature of the contact resistance lies in the measurement not being a truly 4 terminal, it bypasses only the filters in the fridge not the Ti/Au Al contacts.

S2. Growth Map for InAs NWs on the Trench

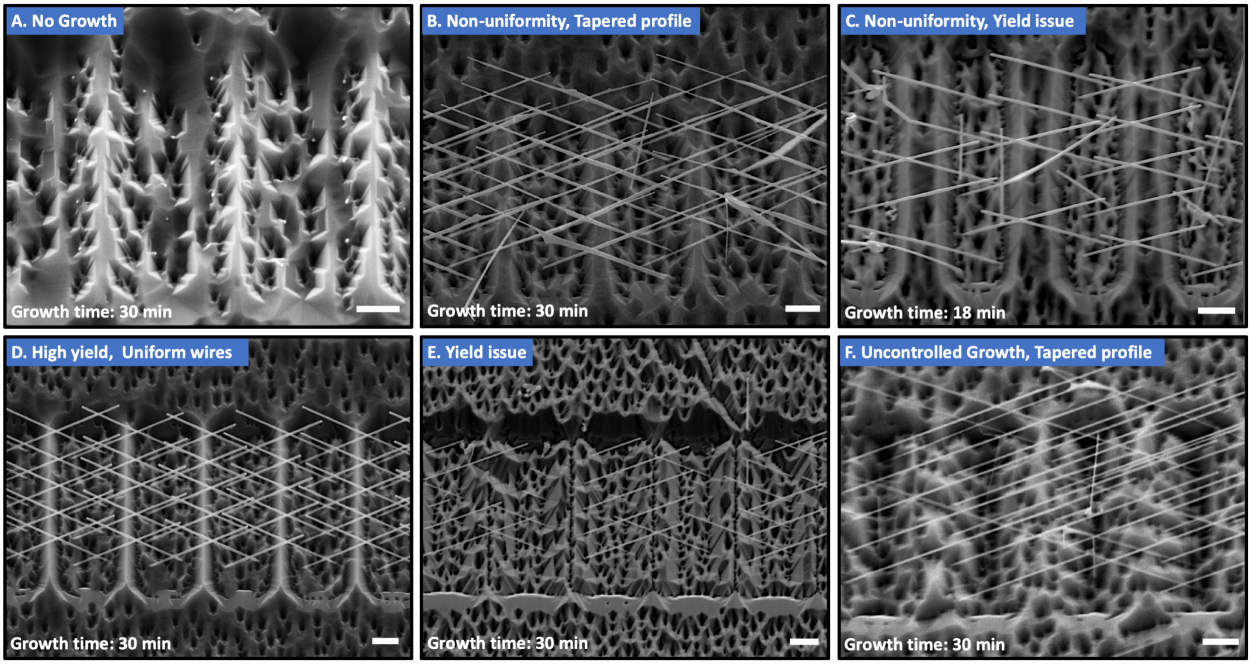

Figure 2: **InAs growth window on the (111)B trenches a**, SEM micrograph of the InAs NWs growth on the trenches in different growth conditions. Region **D** demonstrates the highest yield ($> 90\%$) and uniform NWs growth. Scale bar is 1 μm.

Fig. 2 is the extended demonstration of Fig. 1b in the main text. Starting from region **A**, with growth temperature < 400°C (pyrometer reading) and V/III ratio ~ 10, none of Au seed particles nucleate and grow NWs. Most of the trenches are filled with InAs bulk growth. Reducing the V/III ratio from **A** (in region **B**) exhibits increased the yield of InAs NWs. However, we observe non-uniformity along the wires such as diameter change and tapered profile. Maintaining the V/III ratio we increase the temperature ~ 5°C in region **C** ($\sim$ 405°C). We still observe non-uniformity along the wires with decreased yield. Maintaining the growth temperature, from **C** to region **D** we only increase the V/III ratio $\sim$10, which improves both yield ($> 90\%$) and morphology of the NWs. For instance, the growth time of 30 min results homogeneous $\sim$ 5-5.5 μm long NWs with diameter varied from 70-90 nm depending on the lithography and deposited thickness of the Au seed particles. It is also

possible to grow longer wires maintaining the uniformity in region **D**, however, we choose to grow in length mentioned above considering our shadow design. Post-growth TEM analysis in multiple growth sections of the wafer confirms pure wurtzite (WZ) InAs structures with minimal crystal defects along the individual NW as shown in supplementary 3. We believe this less crystal defects can also be attributed to the high incident materials flux on the angled NW surface, however systematic study is required for proper understanding. Further, if we increase the V/III ratio from region **D** to **F** ($\sim$ 16), we observe uncontrolled NWs length and diameter with a tapered profile. Finally, in **E** with increased growth temperature (more than 20°C from **D**), we start observing yield issue again across the substrate.

S3. Transmission Electron Microscopy of InAs and InSb Nanowire

InAs and InSb NWs are widely used materials for Majorana devices due to the strong spit-orbit coupling and large Landé-g factor [3]. Besides, ballistic transport of electrons is also crucial, which requires high single crystal quality [4, 5]. Post-growth TEM analysis exhibits high-quality monocrystalline wurtzite structure for InAs and zinc blende crystal structure for the InSb segment as shown in Fig 3. Small structural defects are observed at the top of NW near seed particles which can be attributed to the cooling effect. In InSb wires, few layers of transitional defects are also observed between InAs stem and InSb segments. However, these defects do not affect the measurements as the intended NW device segment is defect-free.

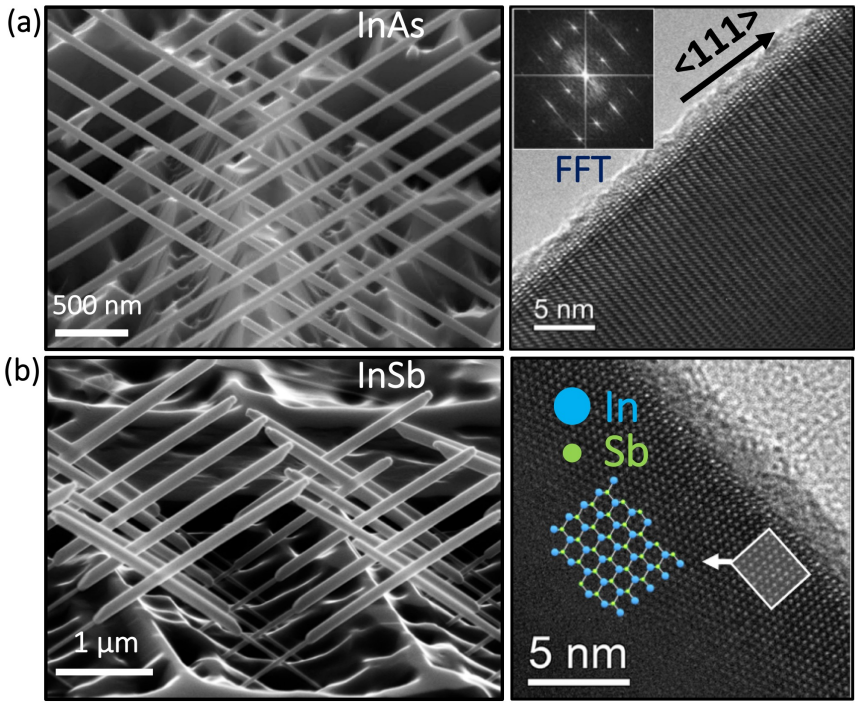

Figure 3: **Monocrystalline semiconductor nanowires.** **a**, Tilted SEM micrograph of InAs NWs on the trenches grown for 30 min. In the right, high-resolution TEM of the wire demonstrating stacking fault-free monocrystalline WZ structure. The inset shows corresponding diffraction pattern. **b**, Tilted SEM micrograph of InSb NWs where 12 min of InAs stem is grown initially and 45 min InSb is grown on top of it. High-resolution TEM is shown in the right demonstrating pure ZB crystal structure along the wire.

S4. Thin Al growth on Semiconductor NWs

For Majorana devices, thin Al film on the wire is crucial to survive high magnetic field without suppressing superconductivity [3, 6]. However, It is challenging to grow homogeneous thin Al on the semiconductor wire as the equilibrium shape of Al on the wire is dewetted droplet [7, 8]. With short deposition time, Al remains grains and does not form uniform layers. We can on the other hand, kinetically force Al to be a continuous film by growing at very low temperature [7, 8]. In low-temperature growth, adatom diffusion length is shorter, which helps to form a film. As shown in Fig. 4, with low temperature in MBE ($\sim -36.2°$C) and very short growth time we manage to grow thin uniform Al film on InAs and InSb NWs. To avoid dewetting in room temperature while taking out, we oxidize (by O_2 venting) the sample (making AlO_x layer) in MBE to lock the Al film and make it stabilized.

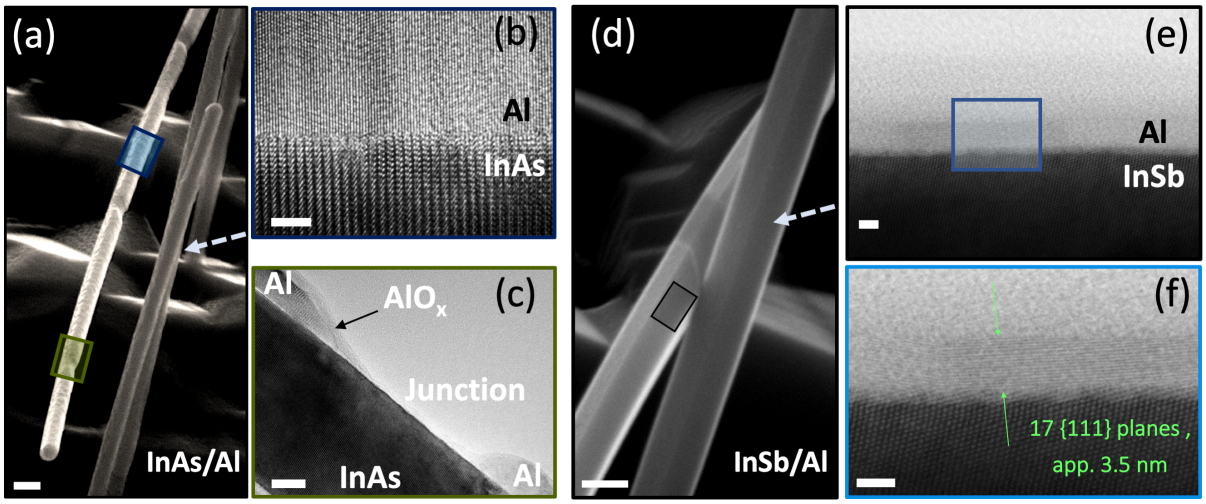

Figure 4: **Thin Al epitaxy on InAs and InSb NWs. a**, 30° tilted SEM image of *in-situ* Al hybridization on InAs NW. Scale bar is 100 nm. Arrow shows the Al deposition direction which is aligned with the substrate such a way that NWs shadow each other. **b**, TEM image of blue highlighted area shows the epitaxy of InAs/Al hybrid (Scale bar is 5 nm). **c**, TEM image from green highlighted area, which shows the clean SU-SE-SU junction (Scale bar is 20 nm). **d**, SEM micrograph of InSb/Al NW with junction. The arrow shows Al deposition direction. Scale bar 100 nm. **e**, Magnified TEM micrograph of InSb/Al epitaxy. **f**, Magnified TEM of blue section shows 3.5 nm thin homogeneous Al layer. Scale bars for **e** and **f** are 2 nm.

S5. Advanced Shadow Schemes for Different Junctions

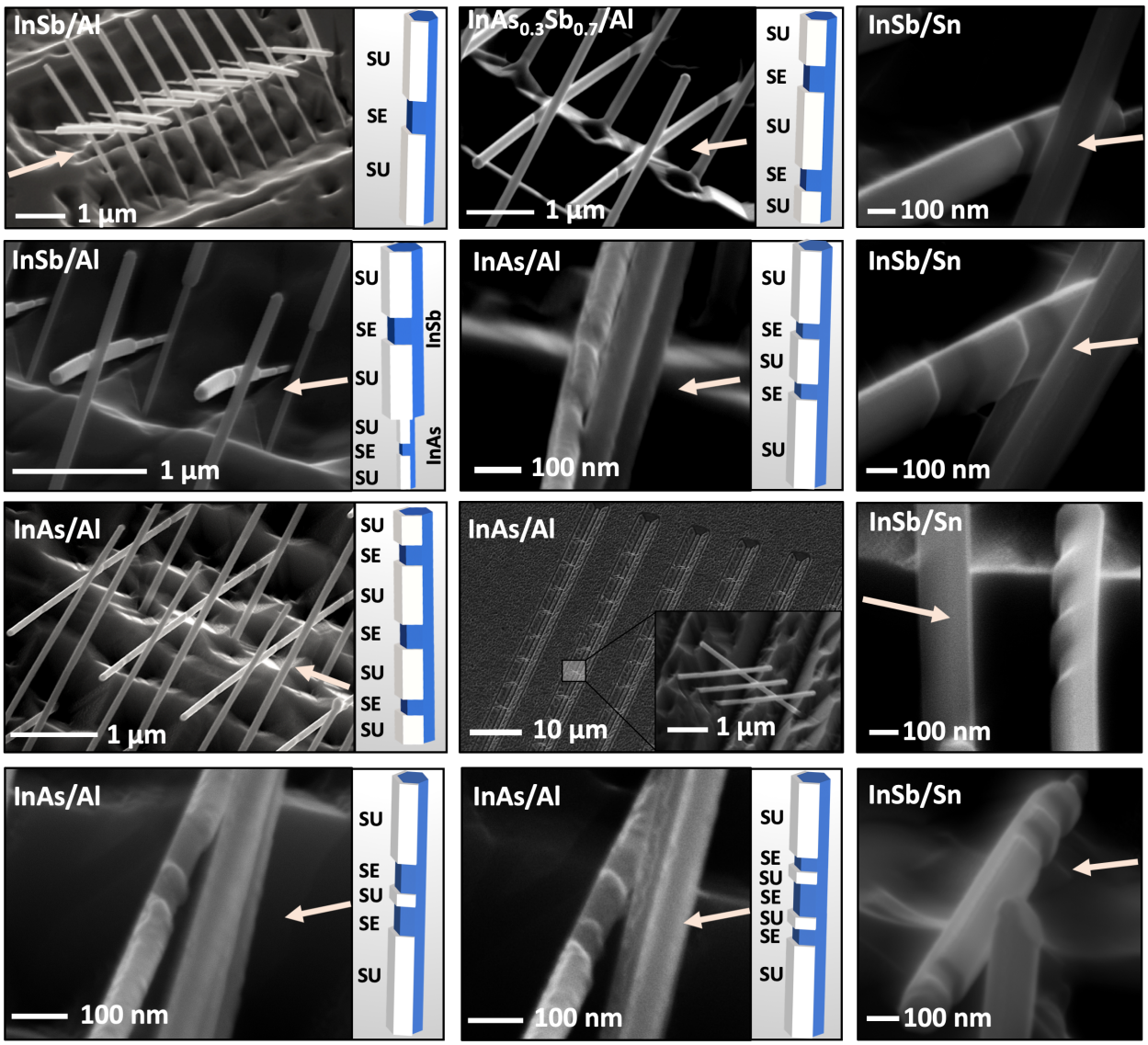

Figure 5: **Shadow schemes.** SEM micrographs and schematic of different shadow junction schemes grown on the trenches. SU deposition direction is shown with arrow.

S6. Tomography and Composition Analysis of $InAs_{1-x}Sb_x$ NWs

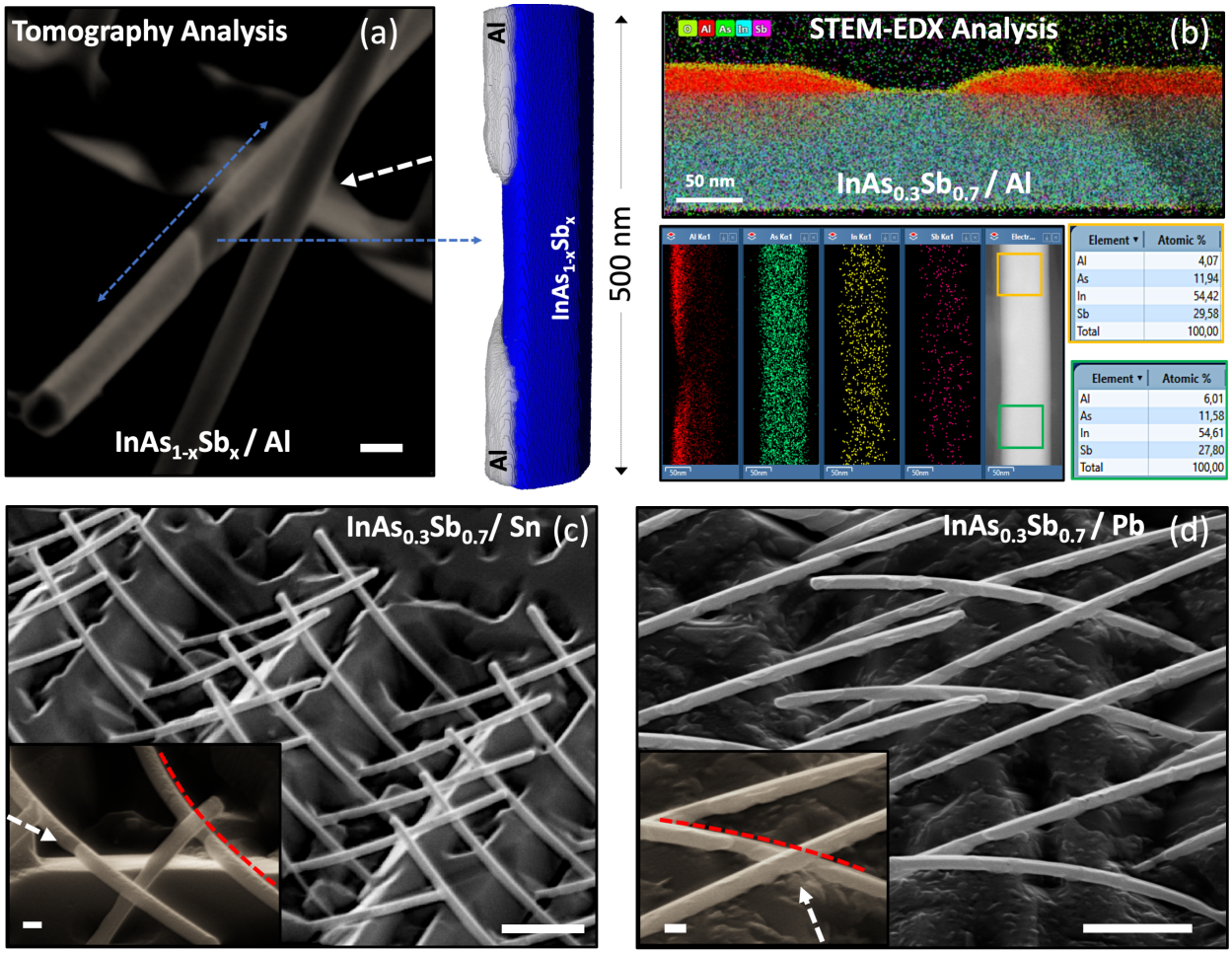

Figure 6: $InAs_{0.3}Sb_{0.7}$ **NWs with different superconductors a**, SEM micrograph of $InAs_{1-x}Sb_x$/Al NW junction. Scale bar is 100 nm. Blue arrow to right is the HAADF-STEM tomography of the NW demonstrating junction morphology. **b**, STEM-EDX of the junction shows In, As, Sb and Al composition. As shown in the bottom, the grown $InAs_{1-x}Sb_x$ NWs consist 30% of As and 70% Sb and the composition remain homogeneous along the individual NW. **c**, $InAs_{0.3}Sb_{0.7}$ NWs with Sn. **d**, $InAs_{0.3}Sb_{0.7}$ NWs with Pb. Scale bar for **c** and **d** are 1 μm. Insets scale bars are 100 nm. All the white arrows in the SEM images show direction of superconductor deposition.

In complementary to the main-text Fig 2 and 3, we also investigate the $InAs_{1-x}Sb_x$ NWs junction quality with STEM tomography as shown in Fig 6 (a). Experimental Details of the tomography are discussed in S1. Here in tomography image, we can see abrupt junction. However, in some cases, we also observe homogeneous 2 facet Al and discontinuous third

facet Al similar to AFM analysis of main-text Fig 3 . This non-uniformity of the SU on NW can be related to the large interwire distances, SU deposition angle with respect to the NW facets and in some cases, inhomogeneous growth of the NW itself. As already discussed, for enhanced spin-orbit interaction, better electrical gatability and convenient device fabrication we aim for $x = 0.7$ Sb concentration in our $InAs_{1-x}Sb_x$ NWs [9]. We confirm the composition with STEM-EDX analysis and shown in Fig. 6 (b). $InAs_{0.3}Sb_{0.7}$/Sn hybrid is shown in Fig. 6 (c) where nominal $\sim$ 20 nm Sn is deposited on wire facet at very low temperature. The continuous thin film of Sn is formed on NW facets, however, rough Sn surface is observed compared to InSb/Sn NWs. Also after Sn growth NWs seems to bend away from the Sn. This bending could be due to the different thermal expansion coefficient between the ternary $InAs_{0.3}Sb_{0.7}$ NW and Sn during temperature increment after NW growth. $InAs_{0.3}Sb_{0.7}$ with continuum Pb hybridization is shown in Fig. 6 (d). Magnified NW and junction segments are shown in Inset, where unlike $InAs_{0.3}Sb_{0.7}$/Sn, $InAs_{0.3}Sb_{0.7}$/Pb demonstrate bending towards the Pb. Such bending can be due to the compressive strain in the interface of $InAs_{0.3}Sb_{0.7}$ and Pb along the NWs, which is also comparable in some cases of InAs/Al interfaces [7].

S7. Disorder in the Etched Junctions

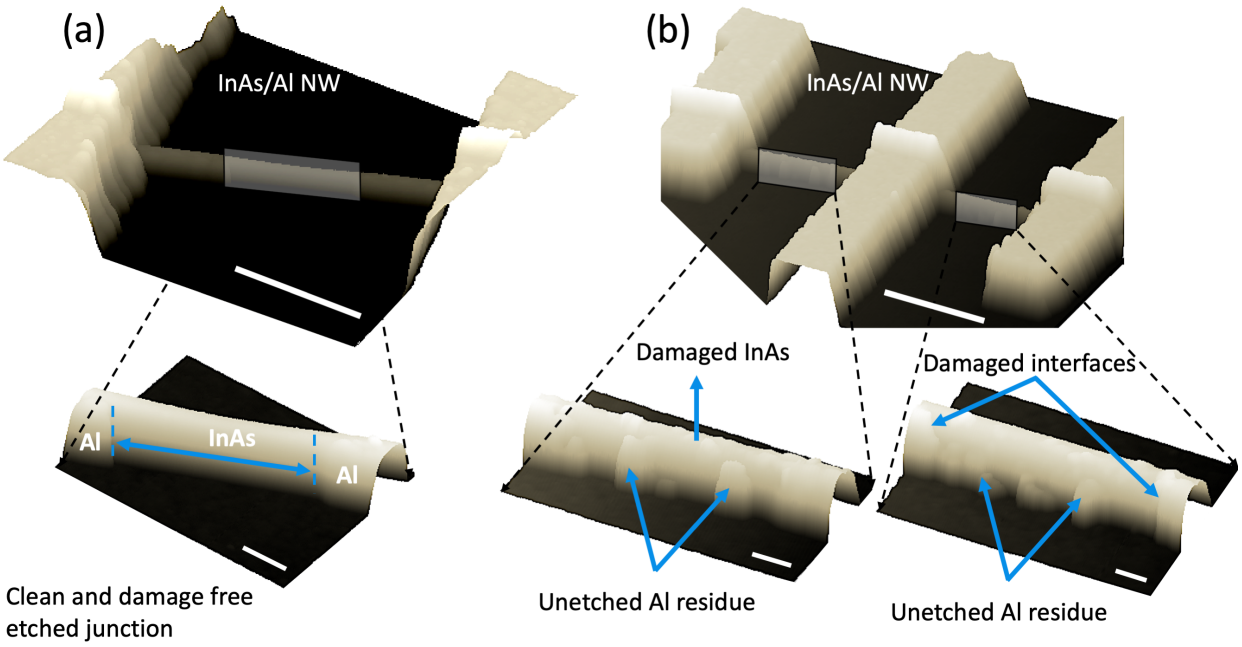

Figure 7: **Post-growth etching of the junctions.** **a**, AFM image of etched InAs/Al NW device (scale bar 500 nm). Zoomed-in junction (scale bar 100 nm) exhibits a disorder-free semiconducting segment. **b**, AFM image of double junctions device (scale bar 500 nm) where magnified segments of the junctions (scale bar 100 nm) exhibit Al residue, rough InAs surface, and damaged SE/SU interfaces.

Examples of etched InAs/Al junction devices are shown in Fig. 7. The etching is performed using standard Transene Aluminum etchants-type D with optimal etch time [6, 10, 11]. In Fig. 7 (a) and (b), both devices are fabricated in the same chip and junctions are etched under the same etching condition. However, the junction in device Fig. 7 (a) is clean and damage-free, whereas junctions in Fig. 7 (b) exhibit incomplete etching and damaged profile. As a result, in the same chip, junctions performance in different devices will be deviated and non-reproducible due to the uncontrolled etching. This phenomenon justifies the statistics of inadequate performances in the etched junctions compare to the shadowed junctions as discussed in the main text. On the other hand, optimized *in-situ* shadow junctions avoid disorders and exhibit high yield reproducible superconductive devices.

S8. Shadowed and Etched Junctions

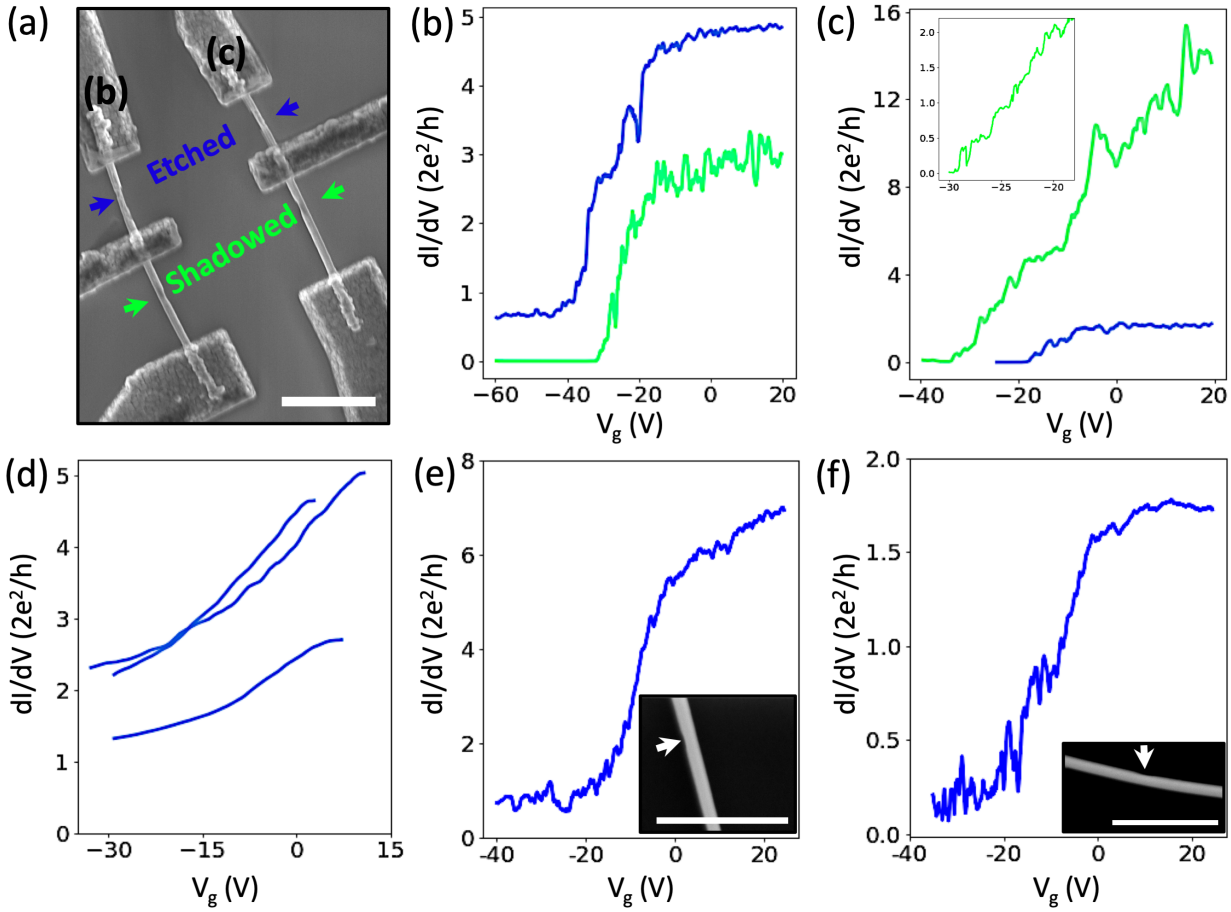

Figure 8: **Electrical measurements of shadow and etched junctions.** **a**, SEM image of NW devices with shadowed and etched junctions in individual wires. Blue colour stands for the etched junctions and green for the shadowed. Measurements are taken in a dilution refrigerator at 20 mK. **b**, The etched junction is not pinched-off and shadowed junction is pinched-off. **c**, Both junctions are pinched-off, whereas the shadowed device shows quantized conductance (inset) for high field (6 T). **d**, The results of the etched junctions obtained from the PPMS at 2 K. None of the junctions are pinched-off within the voltage range. **e**, and **f**, Two shadowed NW junctions that have not pinched-off due to the ambiguous junction region pointed by the white arrows in the relevant SEM images. The scale bars of all the SEM images are 1μm.

S9. Resistance Calculation and Field effect mobility fit

Pinch-off curves are fitted using the formula developed in the ref. [12–14] and also shown below. The mobility values of 16 devices are extracted using the formula fit and the *direct*

transconductance method as described ref [14], and the results we get are in agreement.

$$G(V_g) = (R_I + \frac{{l_J}^2}{\mu C(V_g - V_{th})})^{-1}$$

Here in the formula, R_I is the gate-independent resistance, C is the capacitance calculated from the cylindrical approximation with the correction for hexagonal NWs [15], l_j is the junction length and μ is the field-effect mobility.

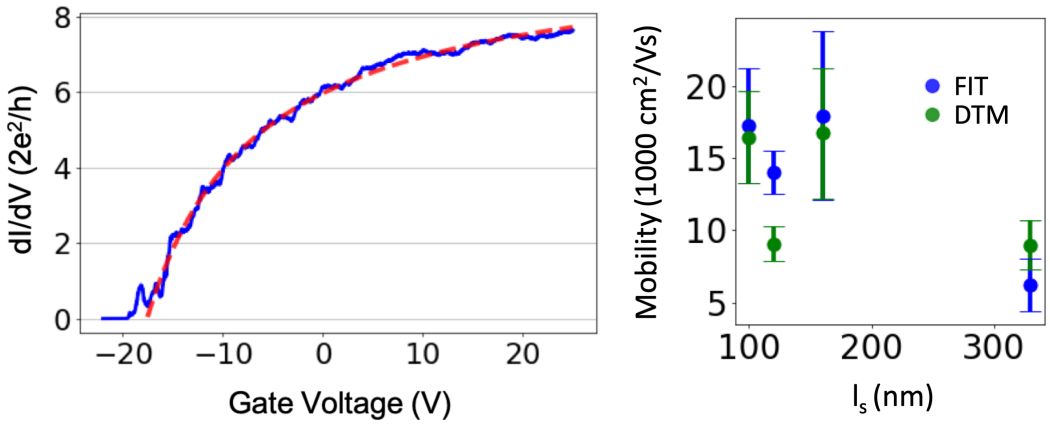

Figure 9: **Fitting of a pinch-off curve.** Blue line: forward sweep of the gate voltage and the evolution of the differential conductance in units of $2e^2/h$. Red dashed line: the fitted model.

The equation above consists of a gate independent term (R_S) and a gate dependent term ($\frac{{l_J}^2}{\mu C(V_g - V_{th})}$). In our device geometry, the first term is more complex than the one described in the ref [12–14]. These are the contact resistance (R_C), the resistance coming from the broadening of the junctions (R_{Δ_b}) and also the resistance of semiconductor-superconductor interface (R_{int}). The effect of the three gate-independent resistances on the junctions are presented in main-text Fig. 3 (i). The contact resistance is extracted from four devices using standard 4-probe measurement technique. The gate-dependent resistance in the equation emerges from the semiconductor segment.

S10. Ballistic Transport on InAs/Al, $InAs_{0.3}Sb_{0.7}$/Al and InSb/Al Junctions

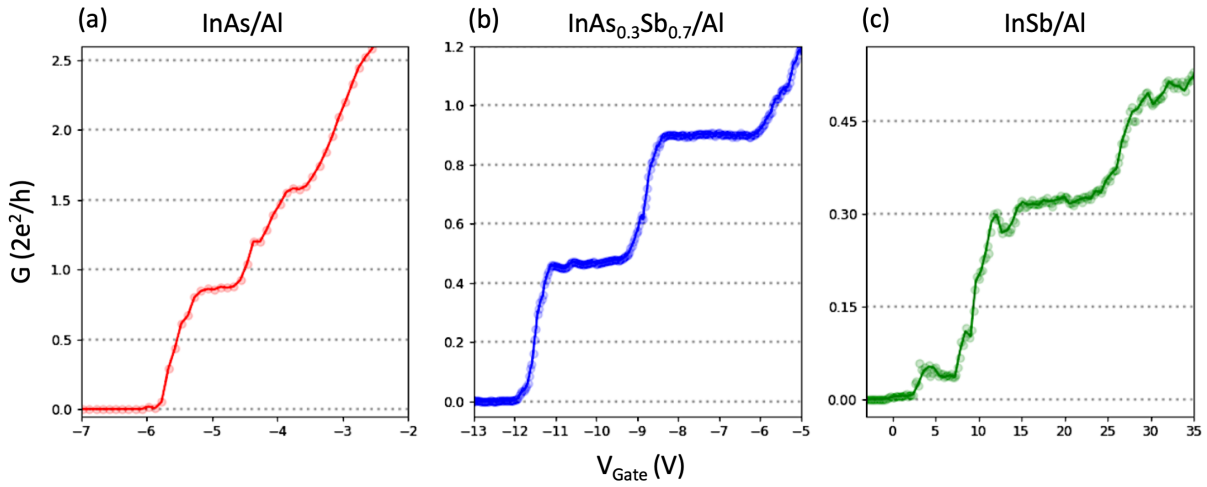

Figure 10: **Quantized conductance on the junctions.** Conductance (G) is drawn as a function of gate voltage for InAs/Al (**a**), $InAs_{0.3}Sb_{0.7}$/Al (**b**) and InSb/Al NW (**c**) junctions. All the plots shown here are measured with 9 T magnetic field, which is applied perpendicular to the NWs. The measurement is done at 2 K and the length of the junction is $\sim$ 100 nm.

Quantized plateaus for all three different NW junctions under magnetic field are observed, as showed in Fig. 10. First, the conductance plateaus do not appear at the exact value of Ne^2/h and differ between the three materials. Second, the conductance plateaus only appear under applied magnetic field, and they become more pronounced with increased magnetic field. Two probe measurements are carried out for all the devices, so other parts in the measurement circuits also contribute to the signals. Apart from that, the difference caused by contact resistance and contact geometry among different materials may also the reason behind the deviation from e^2/h, $2e^2/h$, etc. As can be seen in Fig. 10, for InAs, two plateaus are identified where the first plateau appeared around $2e^2/h$. On the otherhand, for InSb and $InAs_{0.3}Sb_{0.7}$, the plateaus are more close to e^2/h and $2e^2/h$. For both, the position of the plateaus can be attributed to subband splitting under high magnetic field, while for InAs, no splitting of plateaus is observed which needs further investigation. The appearance of

conductance plateaus only under magnetic field may be attributed to the disorder (structural or surface states) induced backscattering, which is suppressed by high magnetic field. Various resonances can also obscure the appearance of quantized plateaus.

S11. Sharp-edge InSb/Sn Junctions

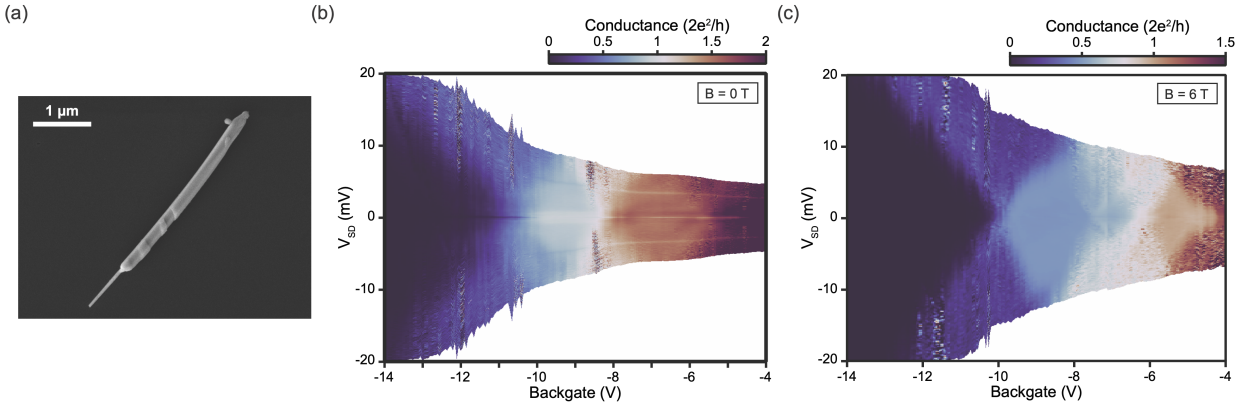

Figure 11: **Electrical measurements of InSb/Sn NW junction. a**, An SEM image of the NW prior to deposition of contacts. Contacts are deposited such that the only center junction is being probed. The measured dimension of this junction is 210 nm. **b**, A two-terminal source-drain measurement is taken at **B**=0 T, while **c**, shows the same measurement taken at **B**=6 T. The source-drain bias (V_{SD}) at the device is extracted for both measurements using the known resistance of the filters and contacts in the fridge. In both sets of data, quantized conductance plateaus are visible, suggesting transport in the junction is ballistic on the order of a few hundred nanometres. As is expected, at zero field the first plateau has a conductance of $2e^2/h$, while at 6 T, spin degeneracy is broken leading to the emergence of a plateau at e^2/h. In the zero-field data, features relating to the superconducting shell are visible near zero bias and as two dips symmetric around zero bias.

For InSb/Sn devices, fabrication procedures are mostly similar to the process described in S1. NWs are deposited on degenerately doped Si wafers with a 300 nm wet oxide. To allow cold processing, the PMMA A4 is vacuum baked for $>$ 1 hour at $P < 5e^{-4}$ mbar instead of baking. Contact materials are 12/180 nm Ti/Au with a 5 minute in-situ Argon milling prior to contact deposition.

S12. Low Temperature ($T \sim 20\,\mathrm{mK}$) Measurements on the Junctions

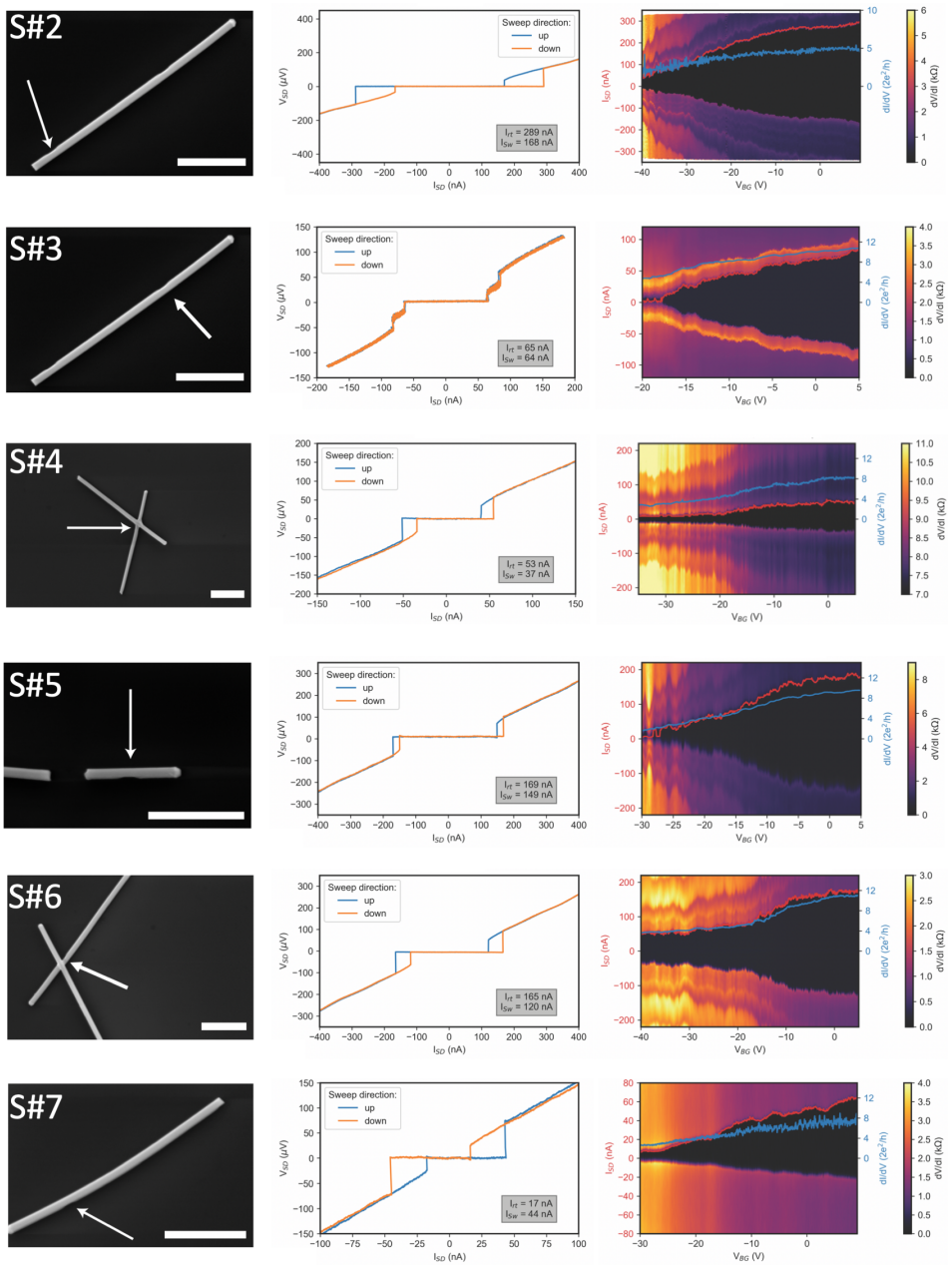

Figure 12: **Supercurrent measurements.** First column of this figure shows the SEM before metallization of the 6 devices shown in Fig. 5 of the main-text. The shadowed region is hinted with an arrow. In the case of the crosses, the merged NW is fully metalized with the corresponding contact in order to avoid floating pieces of SU close to the junction. Second Column indicates the I-V characteristics of the junctions with up and down sweep at V_{bg}= 0 V. In device S#3 we note a presence of a step like feature which qualitatively looks like a Fiske step. The third column shows the differential resistances as a function of applied current and back-gate voltage.

References

(1) Khan, S. A. *(To be Submitted.)*

(2) Liu, Y. *(To be Submitted.)*

(3) Lutchyn, R. M.; Bakkers, E. P. A. M.; Kouwenhoven, L. P.; Krogstrup, P.; Marcus, C. M.; Oreg, Y. *Nature reviews materials* **2018**, *3*, 52–68.

(4) Van Weperen, I.; Plissard, S. R.; Bakkers, E. P.; Frolov, S. M.; Kouwenhoven, L. P. *Nano letters* **2013**, *13*, 387–391.

(5) Saldaña, J. E.; Žitko, R.; Cleuziou, J.; Lee, E.; Zannier, V.; Ercolani, D.; Sorba, L.; Aguado, R.; De Franceschi, S. *Science advances* **2019**, *5*, eaav1235.

(6) Chang, W.; Albrecht, S.; Jespersen, T.; Kuemmeth, F.; Krogstrup, P.; Nygård, J.; Marcus, C. *Nature nanotechnology* **2015**, *10*, 232–236.

(7) Krogstrup, P.; Ziino, N.; Chang, W.; Albrecht, S.; Madsen, M.; Johnson, E.; Nygård, J.; Marcus, C.; Jespersen, T. *Nature materials* **2015**, *14*, 400–406.

(8) Thompson, C.; Floro, J.; Smith, H. I. *Journal of applied physics* **1990**, *67*, 4099–4104.

(9) Sestoft, J. E.; Kanne, T.; Gejl, A. N.; von Soosten, M.; Yodh, J. S.; Sherman, D.; Tarasinski, B.; Wimmer, M.; Johnson, E.; Deng, M.; Nygård, J.; Marcus, C.; Krogstrup, P. *Physical Review. Materials* **2018**, *2*, 044202.

(10) Albrecht, S. M.; Higginbotham, A.; Madsen, M.; Kuemmeth, F.; Jespersen, T. S.; Nygård, J.; Krogstrup, P.; Marcus, C. *Nature* **2016**, *531*, 206–209.

(11) Larsen, T. W.; Petersson, K. D.; Kuemmeth, F.; Jespersen, T. S.; Krogstrup, P.; Nygård, J.; Marcus, C. M. *Phys. Rev. Lett.* **2015**, *115*, 127001.

(12) Kim, S.; Nah, J.; Jo, I.; Shahrjerdi, D.; Colombo, L.; Yao, Z.; Tutuc, E.; Banerjee, S. K. *Applied Physics Letters* **2009**, *94*, 062107.

(13) Gül, Ö.; Van Woerkom, D. J.; van Weperen, I.; Car, D.; Plissard, S. R.; Bakkers, E. P.; Kouwenhoven, L. P. *Nanotechnology* **2015**, *26*, 215202.

(14) Zhong, H.; Zhang, Z.; Xu, H.; Qiu, C.; Peng, L.-M. *Aip Advances* **2015**, *5*, 057136.

(15) Wunnicke, O. *Applied Physics Letters* **2006**, *89*, 083102.