Shadow lithography for *in-situ* growth of generic semiconductor/superconductor devices: Supplementary Information

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SUPPLEMENTARY SECTION 1. FABRICATION OF SHADOW LITHOGRAPHY SUBSTRATES.

The fabrication process is schematically illustrated in Figure S1. Epi-ready InAs (111)B oriented wafers were capped with 100-150 nm of SiOx by plasma-enhanced chemical vapour deposition (Fig. S1a). Photoresist (AZ1505) was spun onto this surface, and a custom pattern exposed using a Heidelberg μPG501 LED writer. Electron beam lithography (EBL) is also suitable. After resist development and a soft post-bake (5 mins at 145°C), buffered hydroflouric acid (6% in H_2O) was used to etch the SiOx (Fig. S1b). Bridge widths down to $W = 400$ nm – less than the optical lithography resolution limit – were achieved by controlled overetching. The resist was removed, and the InAs etched using $C_6H_8O_7$(40%):H_3PO_4(80%):H_2O_2, with the SiOx acting as etch mask (Fig. S1c). The result is a wafer-scale shadow lithography pattern, as shown in Fig. S2.

The substrate was then covered by a 15 nm thick Al_2O_3 layer using atomic layer deposition, which protects the bridges in subsequent acid-based cleaning steps (optional). Catalyst particles were defined by EBL, using a PMMA A4.5 (lower) and copolymer EL13 (upper) resist stack. Circular openings with diameter ~ 100 nm were made proximal to each bridge. Transene D was used to remove the Al_2O_3, and hydroflouric acid to clean the exposed InAs surface. 10 nm Au was deposited using e-beam evaporation, leaving catalyst particles after lift off (Fig. S1d). The purpose of the copolymer EL13 is to coat the bridges during Au deposition and prevent Au sticking to them; the exposed regions in the copolymer EL13 are much wider than in the PMMA after development and therefore do not impact the definition of the catalyst particles.

The substrate was loaded into the MBE chamber after cleaning for 5 sec using hydroflouric acid, and nanowires were grown as described in the Methods section (Fig. S1e). Finally, the substrate was transferred under ultra high vacuum to a general purpose metal evaporation chamber, with freely rotatable sample holder. The sample holder can be cooled to approx -150°C using liquid nitrogen. The superconductor layers (Al, Ta, Nb, V) were deposited using e-beam evaporation at a fixed angle such that the bridges produced shadowed regions on the desired section(s) of the nanowires (Fig. S1f)

While the described process was designed specifically for InAs nanowire growth, using other materials and etchants would enable the growth of different semiconductors. Growth of

InSb is trivially related, since growth of a short InAs stem typically precedes InSb nanowire growth[1]. A method for producing SiN bridge structures on silicon substrates has been presented in Ref. 2. This would allow the platform to be applied to growth of many nanowire materials, including silicon, germanium[3], GaAs[4], and GaN[5]. Similarly, the etches used in Ref. 6 for InP coated with SiOx would produce bridges on these substrates with the appropriate lithography, enabling phosphide- and antimonide-based nanowire growth. Naturally, the semiconductor growth should be done in a vacuum system where deposition of the superconductor is possible without breaking vacuum after growth. Alternatively, hydrogen cleaning[7] immediately before superconductor deposition appears sufficient to generate a pristine surface and hard superconducting gap[6]. Exploring this option for materials beyond InAs and InSb[6,7] would be very interesting.

SUPPLEMENTARY SECTION 2. GEOMETRIC CONSIDERATIONS.

Figure S3a illustrates how bridge width, W, separation, S_{B}, SiOx thickness, t, and deposition angle, θ determine l_{SE} and l_{SU}, the length of the semiconducting (i.e. shadowed) and superconducting (i.e. not shadowed) segments, respectively. The equations read $l_{\mathrm{SE}} = W\tan(\theta) + t$ and $l_{\mathrm{SU}} = S_{\mathrm{B}}\tan(\theta) - t$. Given θ and t are fixed for each substrate/deposition, w and S_{B} are the free variables used to define l_{SE} and l_{SU}.

This is the ideal case; there are additional factors that contribute to l_{SE} and l_{SU} that are best determined experimentally. Firstly, material may grow on the bridges during semiconductor growth, depending on the selectivity at the required growth conditions (temperature, time, flux, etc). This increases W and t, thereby increasing l_{SE} and decreasing l_{SU}.

Secondly, the finite radius of the deposition source, r, influences the abruptness and morphology of the SU tails as depicted in Fig. S3b (see also Fig. 2 of main text). Each point of the deposition source generates material flux over a wide, solid angle. The orange and pink coloured areas in Fig. S3b represent the material flux originating from points $R_{1,2}$ at either extremity of the source. The shadow mask causes different terminating edges for material originating from each position, indicated by the dashed lines. This effect, taking into account all points across the source, is a gradual decrease in deposited material thickness across the tail, with length l_{t}. For small deposition angle θ, $l_{\mathrm{t}} \sim 2rS_{\mathrm{NW}}/S_{\mathrm{S-S}}$ where S_{NW} is the distance between the nanowire and oxide barrier, and $S_{\mathrm{S-S}}$ is the source-substrate

separation. Additionally, the non-linear dependence of flux on r – arising since the e-beam is focussed at the center of the source – generates a non-linear thickness profile in the tail. The dimensions of our evaporation chamber and substrates yields estimated $l_{\mathrm{t}} = 100 - 200$ nm.

Thirdly and finally, cluster diffusion plays an increased role for materials with a lower heat of vaporisation, such as Al. For Nb and Ta, the high heat of vaporisation results in lowered mobility on the InAs surface and therefore the tail profile of the deposited material is determined largely by the adatom flux gradient due to the finite source size and shadow geometry. Adatoms for other materials such as Al remain mobile, and may form a crystalline, epitaxial film that does not have a geometrically defined l_{t} (Fig. 2 of the main text). Measuring the effect of all three of these factors allowed us to accurately estimate and predict the resultant l_{SE} and l_{SU} for our shadow mask designs.

SUPPLEMENTARY SECTION 3. ADDITIONAL STRUCTURAL CHARACTERISATION.

Transmission electron micrographs highlighting the large-scale structure of each material are presented in Supplementary Figure S4. Fig. S4a illustrates the robust crystal ordering of Al films. This is evident in the Fast Fourier Transform (FFT) of Fig. S4a, shown in Fig. S4b, with six, well defined peaks associated with the FCC Al crystal highlighted by the arrows. The remaining peaks are associated with the wurtzite InAs nanowire. By contrast, Ta and Nb (Figs S4c/e) formed nanocrystalline or amorphous films, with a columnar structure oriented along the angle of deposition[8]. Note that for this ~ 20 nm thick Ta film, the nano-sized grains are no longer visible in the TEM image, as they were for the image of the 5 nm thick film in Fig. 2b of the main text. The FFT in Fig. S4d, corresponding to the image in Fig. S4c again shows InAs-related peaks, but no evidence of any other crystal structure. Instead, a low intensity ring is present, indicated by the arrow, suggesting the presence of an amorphous/nanocrystalline structure. The ring feature is more prominent in the selected area diffraction signal for Nb (Fig. S4f).

SUPPLEMENTARY SECTION 4. ETCH DAMAGE ON EPITAXIAL INAS/AL NANOWIRES.

Figure S5 shows SEMs of epitaxial InAs/Al nanowires after etching of the Al shell using Transene Al etchant type D, the standard etchant. In the ideal case, the aluminium is selectively removed, as in Fig. S5a. However, we routinely observe variations in etch quality. Figs S5b,c show images of nanowires that were processed in parallel, on the same chip as that in Fig. S5a. In Fig. S5b, residual Al was left within the etch window, suggesting the etch was incomplete. The opposite case is shown in Fig. S5c where the InAs surface was damaged. Fig. S5d shows another example of InAs surface damage from a separate chip but with nominally identical processing. Both incomplete etching and InAs surface damage will cause device instability, irreproducibility, and a low yield of superconducting devices. This highlights the benefits provided by shadow lithography, where no residue or damage is evident, leading to the high stability and yield discussed in Figs 3 and 4 of the main text.

SUPPLEMENTARY SECTION 5. GAP HARDNESS VS V_{g}

Charaterising induced superconductivity using peak hardness values, $G_{\mathrm{N}}/G_{\mathrm{S}}$, is common in literature, however a single value provides limited information since $G_{\mathrm{N}}/G_{\mathrm{S}}$ also depends on the tunnel barrier properties[9–11]. Figure S6a shows the bias spectroscopy measurement presented in Fig. 3b of the main text, and a corresponding measurement of $G_{\mathrm{N}} = G(V_{\mathrm{sd}} = -0.4\ \mathrm{mV})$ and $G_{\mathrm{S}} = G(V_{\mathrm{sd}} = 0\ \mathrm{mV})$ in Fig. S6b. To ensure an accurate measurement, we took $G_{\mathrm{S}}(G_{\mathrm{N}})$ as an average of 2000(100) individual measurements at each V_{g}. At $V_{\mathrm{g}} = -10\ \mathrm{V}$, the device is in deep pinch-off, providing a measurement of the noise floor $\sim 10^{-4}\ 2\mathrm{e}^2/\mathrm{h}$. The gap hardness, $G_{\mathrm{N}}/G_{\mathrm{S}}$ vs V_{g} is plotted in Fig. S6c, having subtracted the noise floor from G_{N} and G_{S}. For most of the studied range, $G_{\mathrm{N}}/G_{\mathrm{S}} = 50 - 110$ (highlighted by dashed lines), with peaks occurring that are likely associated with variations in properties of the tunnel barrier. We find a peak value of 350.

SUPPLEMENTARY SECTION 6. EXTENDED SPECTROSCOPY DATA RELATED TO FIGURE 3 OF THE MAIN TEXT.

Figures S7,S8,S9 show the bias spectroscopy for each device presented in Figure 3 of the main text. Each Al-coated (Fig. S7) and Ta-coated (Fig. S8) device apart from T5 device featured a hard gap over an extended V_{g} range. The white line in each plot shows the gate voltage at which the line traces in Fig. 3d,e of the main text were taken. The data in Fig. 3f,g of the main text (niobium) were extracted from the data in Fig. S9, at the V_{g} and V_{sd} settings indicated by the coloured lines.

SUPPLEMENTARY SECTION 7, CRITICAL TEMPERATURE AND FIELD FOR TANTALUM.

In addition to measuring the induced superconducting gap using spectroscopic hybrid devices, the properties of tantalum films were studied using two geometries shown in Fig. S10a,b. Firstly, four-point probe measurements of an unpatterned, 20 nm thick Ta film on a nanowire (Fig. S10a) were used to determine the critical field and temperature of the film itself. A constant current, I, was applied to one end of the nanowire, and the voltage drop V between the two inner probes was measured. Measurements were normalised to the normal state resistance, $R_{\mathrm{N}} = R(T = 3K)$. Fig. S10c shows $R(B_{\perp})/R_{\mathrm{N}}$ exhibits a critical field of $B_{\perp}^{\mathrm{Ta}} \sim 3.5$ T, much higher than the perpendicular critical field of Al with comparable thickness, typically ~ 100 mT[9].

Figure S10d shows $R(T)/R_{\mathrm{N}}$ exhibiting a critical temperature $T_{\mathrm{C}} = 0.7$ K of the nanowire. While this T_{C} is consistent with the gap $\Delta^{\mathrm{Ta}} = 0.13$ meV observed in Fig. 3e of the main text, it is much lower than $T_{\mathrm{C}} = 4.5$ K of bulk Ta. This is expected since for tantalum, T_{C} is reduced with decreasing film thickness[12]. To confirm this trend, we deposited thin films with 20 nm and 100 nm thickness on InAs substrates (dimensions $\sim 4 \times 1$ mm, Fig. S10b). Measurements on these films showed a $T_{\mathrm{C}} = 0.7$ K and 2.7 K for the 20 nm and 100 nm films, respectively (orange and red traces in Fig. S10d).

SUPPLEMENTARY SECTION 8. JOSEPHSON JUNCTION MEASUREMENTS.

An important use of hard-gap hybrids is in gate-tunable Josephson junctions (JJs)[13–15]. These are realised in the shadow platform with a single bridge, as in Fig. 1e of the main text. Figure S11 presents results of low-temperature measurement of a shadow-JJ device. The map of differential resistance, dV/dI vs. V_g and source current I shows a zero resistance regime at low I with finite dV/dI emerging above a gate voltage-dependent critical current, I_C[16]. Increasing V_g results in an overall increase of I_C due to the decreasing resistance. The additional reproducible non-periodic modulation in I_C is due to interference leading to universal conductance fluctuations[16]. Both the qualitative behaviour and the magnitude of I_C is comparable to conventional hybrids, showing the the shadow JJ may replace conventional nanowire JJ in superconducting electronics, thus simplifying fabrication schemes, increasing the yield and improving reproducibility.

SUPPLEMENTARY SECTION 9. KINKED NANOWIRES

Kinked nanowires are obtained by growing a standard nanowire, interrupting growth and changing the conditions to destabilise the catalyst particle[17,18]. This causes the catalyst to rest on one of the six side facets such that continuing growth produces a branch parallel to the substrate. These nanowires are useful as the starting point for more complicated nanowire networks[18–20], as well as providing access to a different InAs crystal phase, since the branch crystallises as cubic zinc blende[17,18]. Figure S12a illustrates the bridge concept applied to kinked nanowires. The branch section is grown such that it passes underneath a bridge, and the metal deposited directly perpendicular to the substrate. An SEM of a kinked nanowire patterned in tunnel probe geometry with vanadium SU layer is shown in Fig. S12b.

SUPPLEMENTARY SECTION 10. LARGE SCALE FABRICATION.

Fundamental research applications of nanowires such as in this work typically proceed by breaking nanowires from the growth substrate and transferring them to a separate, device substrate where they lie in a lateral position. While this simplifies fabrication procedures for investigating a handful of nanowires, it is severely limited with regard to scaling up to large

arrays. Instead, the preference for large scale fabrication is to process device arrays with the nanowires still on the growth substrate, since they are already perfectly arrayed[21–23].

Figure S13 provides a suggested process flow marrying processes already developed for vertical transistor fabrication[21–23] with concepts introduced in this paper. The bridge platform is fabricated as described above, and nanowires grown as normal, before transferring under vacuum into the metal deposition chamber. The first, shadowed metal/superconductor evaporation creates the ohmic contacts and leaves an exposed semiconductor region (Fig. S13a). The nanowire is then conformally coated in an oxide or other dielectric (Fig. S13b). A second metal is deposited from a shallow angle (θ_3) such that only the top part of the nanowire is left exposed (Fig. S13c). This layer will act as the gate. After this step the substrate can be removed from the growth chamber for connecting the top ohmic contact. To so do, a filling layer – e.g. HSQ (hydrogen silsesquioxane)[24], benzocyclobutene (BCB)[23], photoresist[22] or other polymer[21] – can be spun on, to a height where only the top section of the nanowire is exposed (Fig. S13d). The exposed portion of the oxide/dielectric on the nanowire – and the bridges, which are now no longer necessary – can be etched away (Fig. S13e). A final, *ex-situ* metal deposition makes contact to the *in-situ* deposited metal on the top ohmic contact. The bottom ohmic and gate layers can be contacted away from the device by etching through to each layer.

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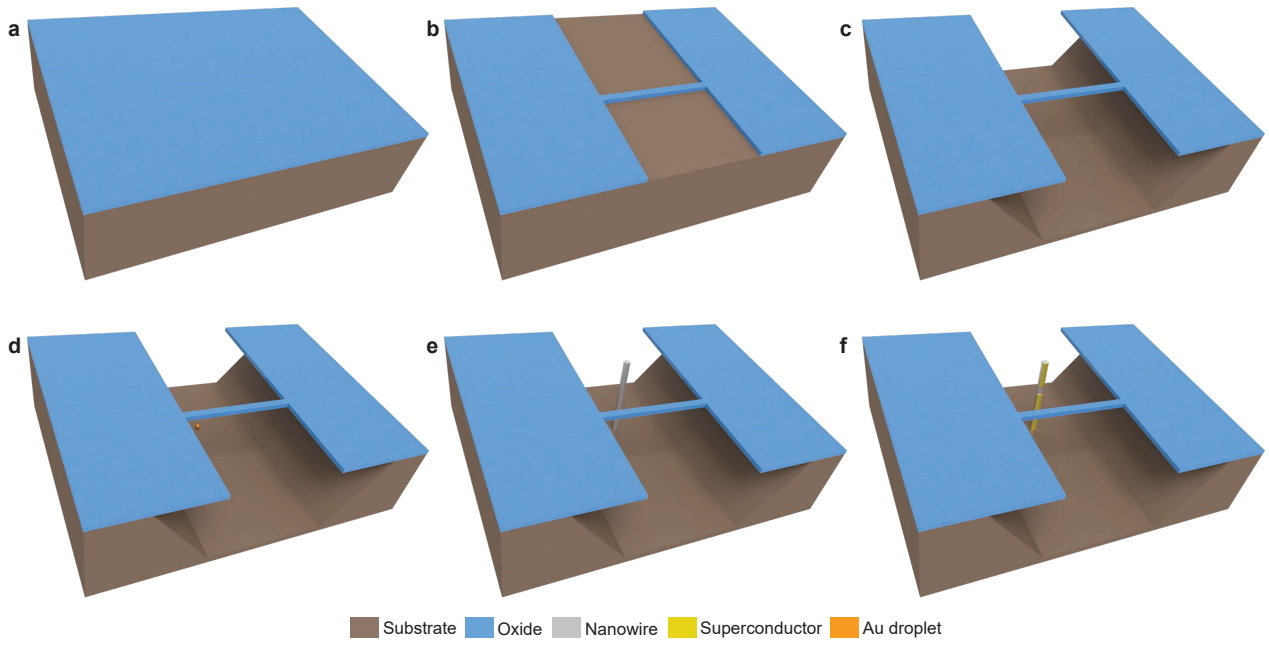

Figure S1. Fabrication process schematics. See text for detailed description of each step.

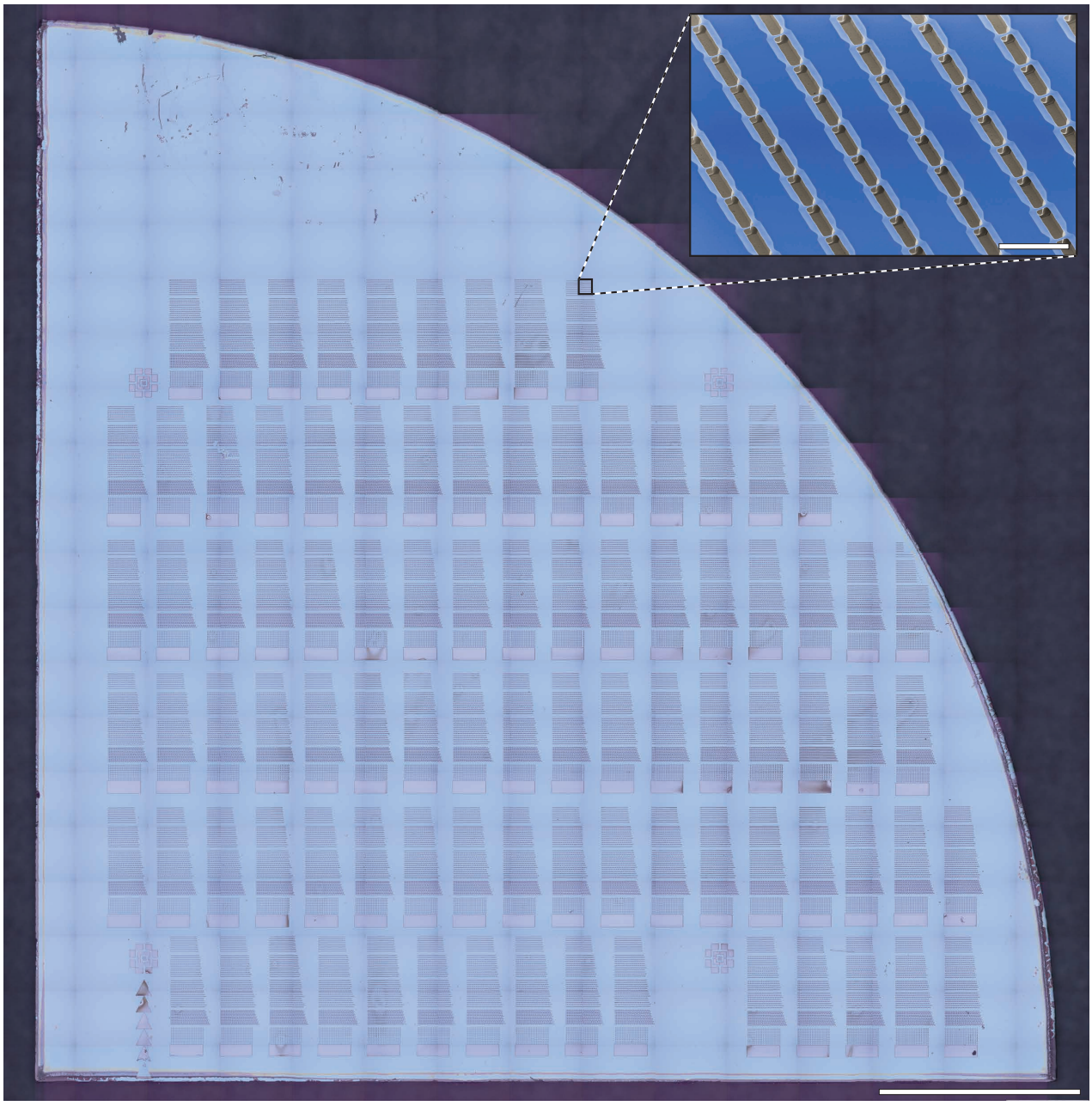

Figure S2. Overview image of finished substrate with shadow mask. Each row is a row of trenches with overhanging bridges (inset). Scale bars on main image and inset represent 5 mm and 50 μm, respectively.

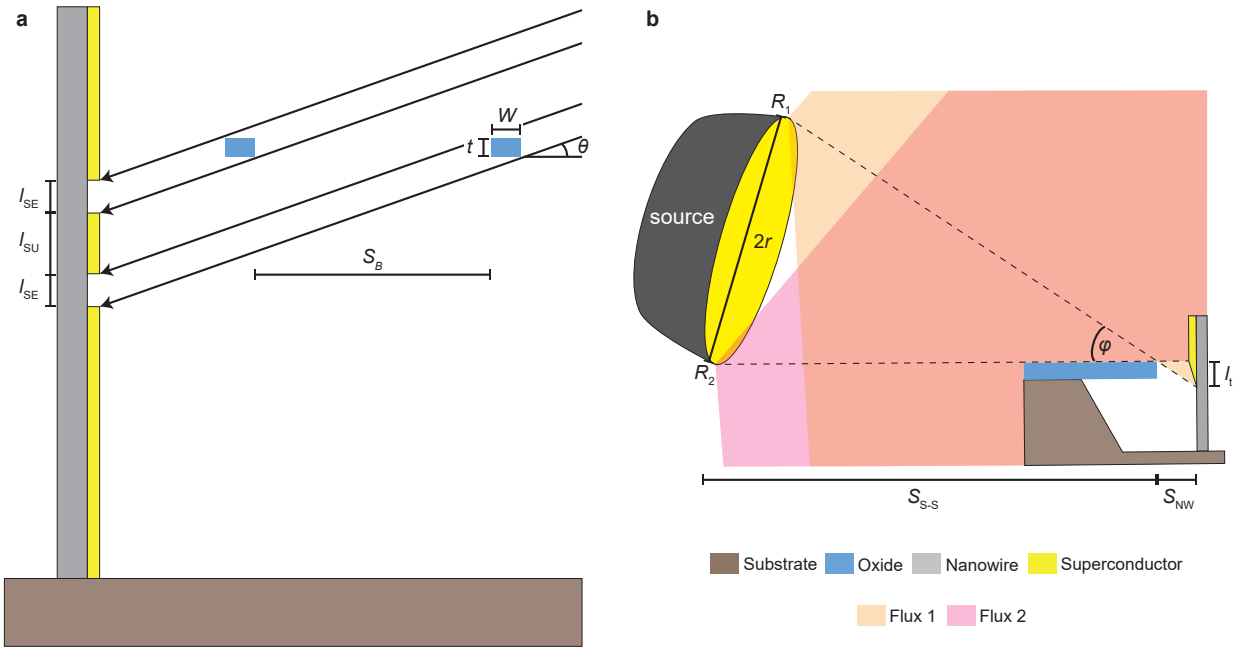

Figure S3. Schematics illustrating geometric considerations in shadow lithography. **a**, Deposition angle θ and bridge dimensions determine semiconductor and superconductor segment lengths according to $l_{\mathrm{SE}} = W\tan(\theta) + t$ and $l_{\mathrm{SU}} = S_{\mathrm{B}}\tan(\theta) - t$. **b**, The finite size of the deposition source is expected to result in SU tails with length $l_{\mathrm{t}} \sim 2rS_{\mathrm{NW}}/S_{\mathrm{S-S}}$. In practice, material diffusion also impacts this parameter.

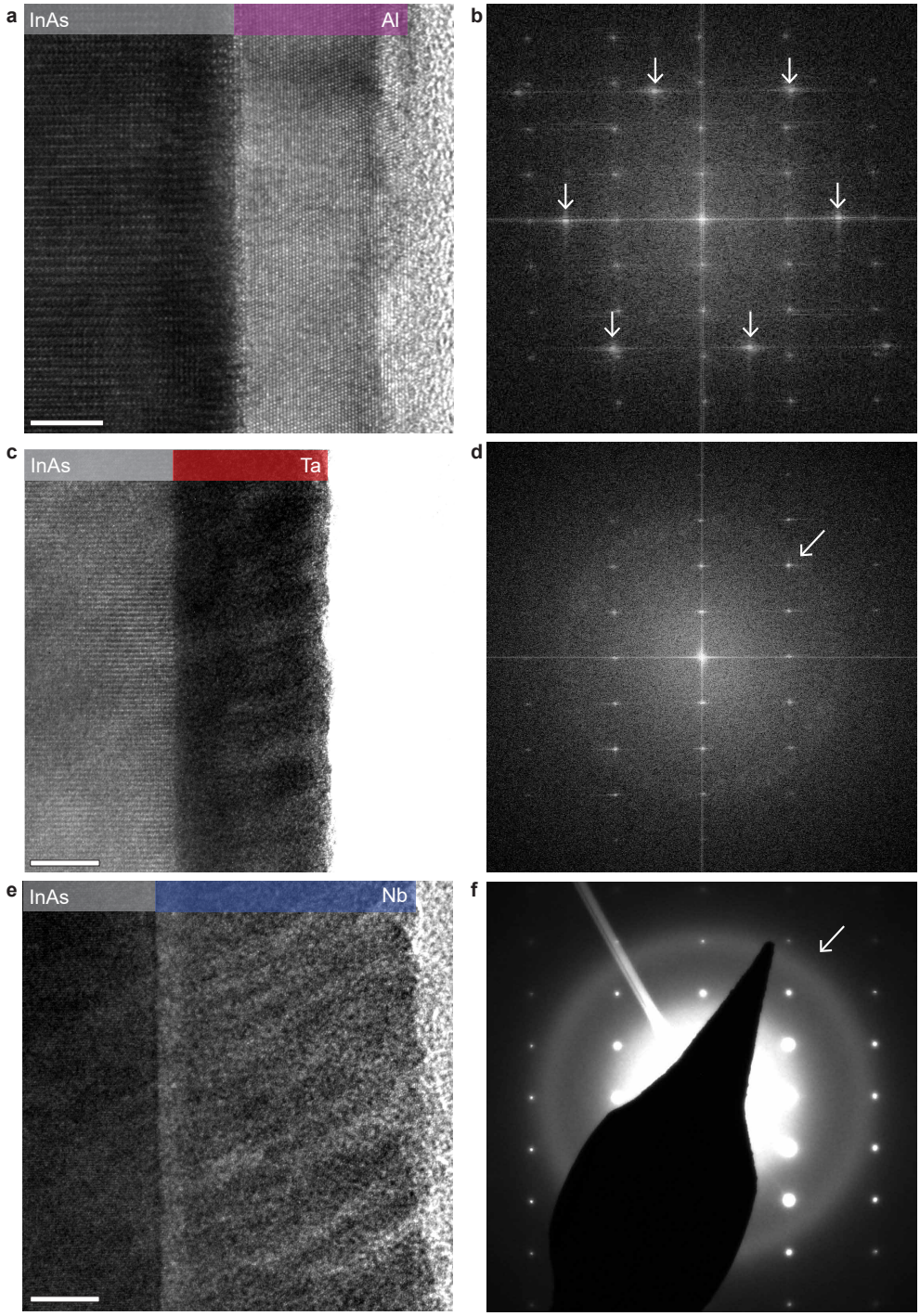

Figure S4. **a,c,e**, High resolution TEM and corresponding **b,d**, fast fourier transform (FFT) or **f**, selected area diffraction for Al/InAs, Ta/InAs and Nb/InAs hybrids. Al-related crystal peaks highlighted by arrows in **b**. The ring associated with the amorphous/nanocrystalline superconductor is indicated by arrows in **d,f**. Scale bars represent **a**, 5 nm, **c,e**, 10 nm.

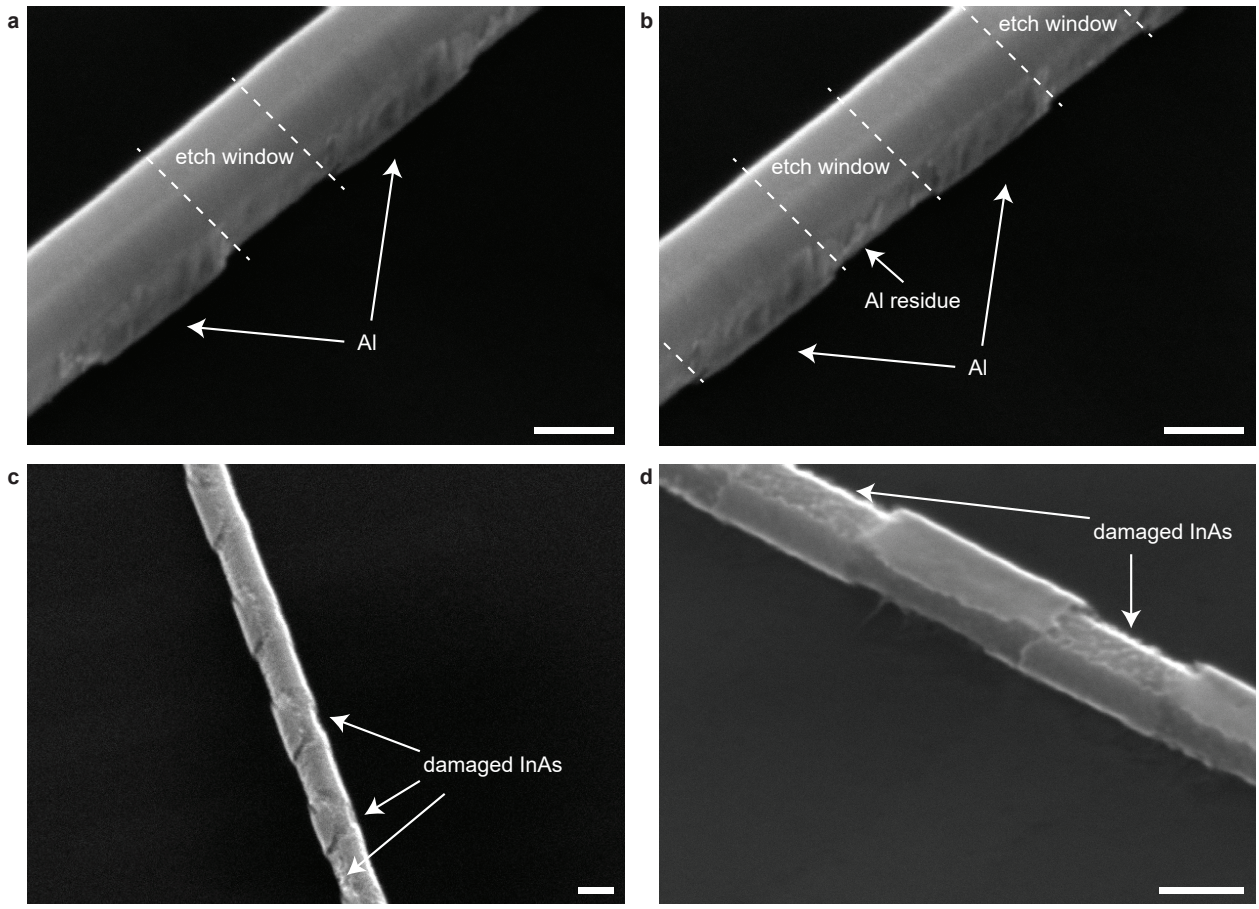

Figure S5. InAs/Al nanowires etched with transene D. **a**, An ideal case where the etch region is free of Al, and no damage was caused. **b**, Remnant Al inside etch windows. **c-d**, Damage to the InAs as a result of overetching. Scale bars represent 100 nm.

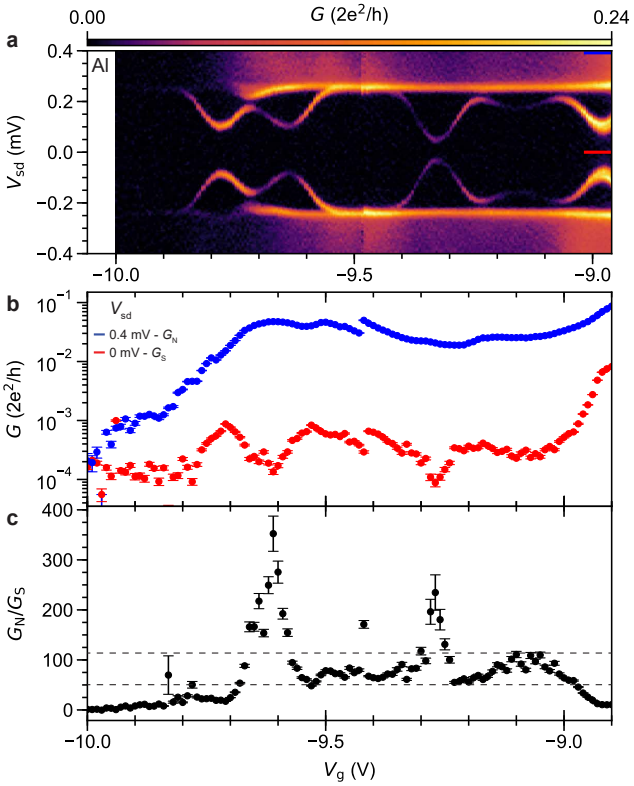

Figure S6. **a**, Bias spectroscopy presented in Fig. 3b of the main text. **b**, Normal state and superconducting state conductance, G_{N} (blue) and G_{S} (red) corresponding to the data in **a**, recorded as described in the text. **c**, Hardness, $G_{\mathrm{N}}/G_{\mathrm{S}}$ calculated from the data in **b**. Dashed lines are guides highlighting that hardness was $G_{\mathrm{N}}/G_{\mathrm{S}} = 50 - 110$ over most of the measured V_{g} range.

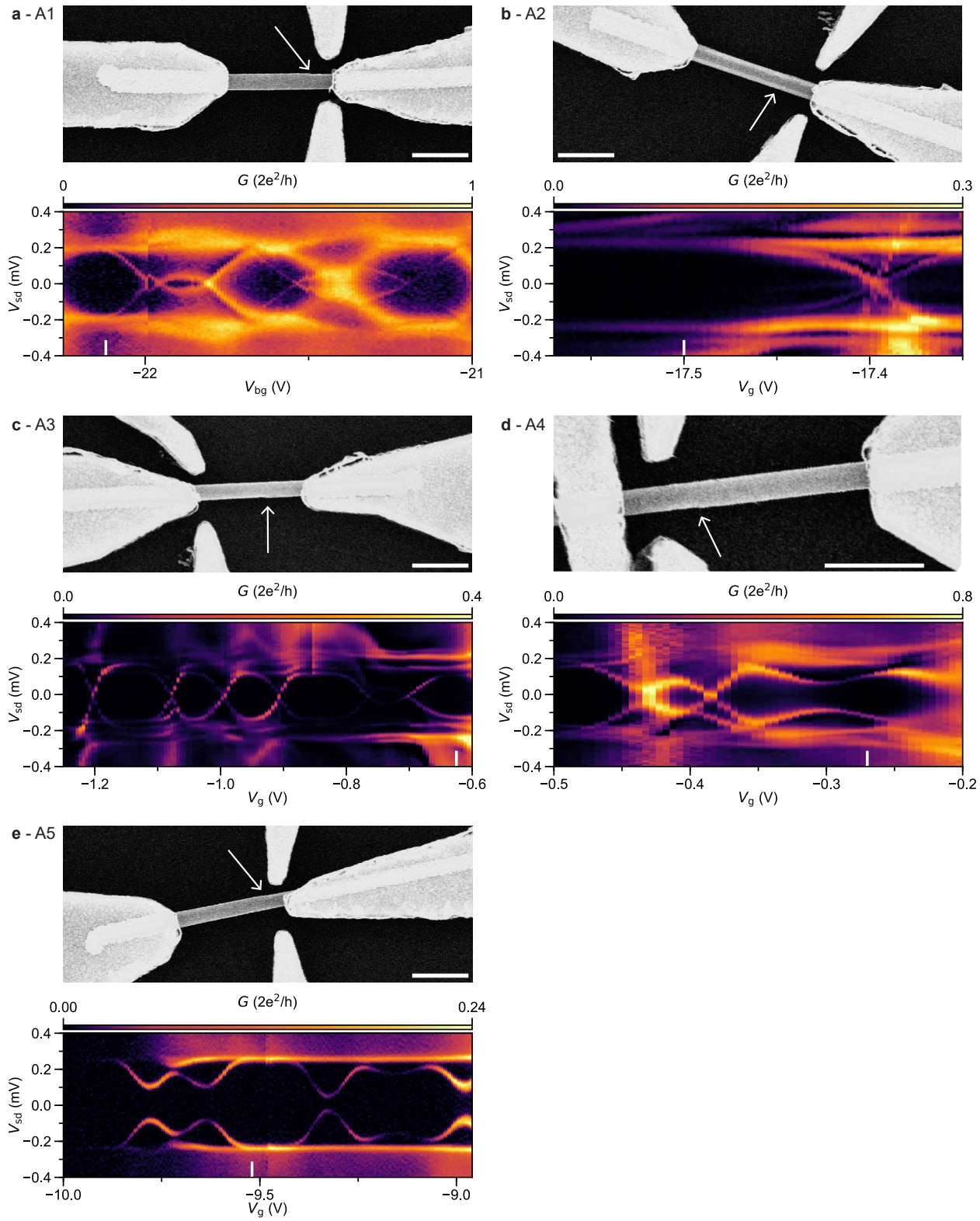

Figure S7. SEM and bias spectroscopy for devices in main text Fig. 3d (Al coated, 8 nm thick). The arrows in each SEM image indicate the shadow-defined Al edge. White lines in each spectroscopy panel show the V_g setting for line traces in main text Fig. 3d. Scale bars represent 500 nm.

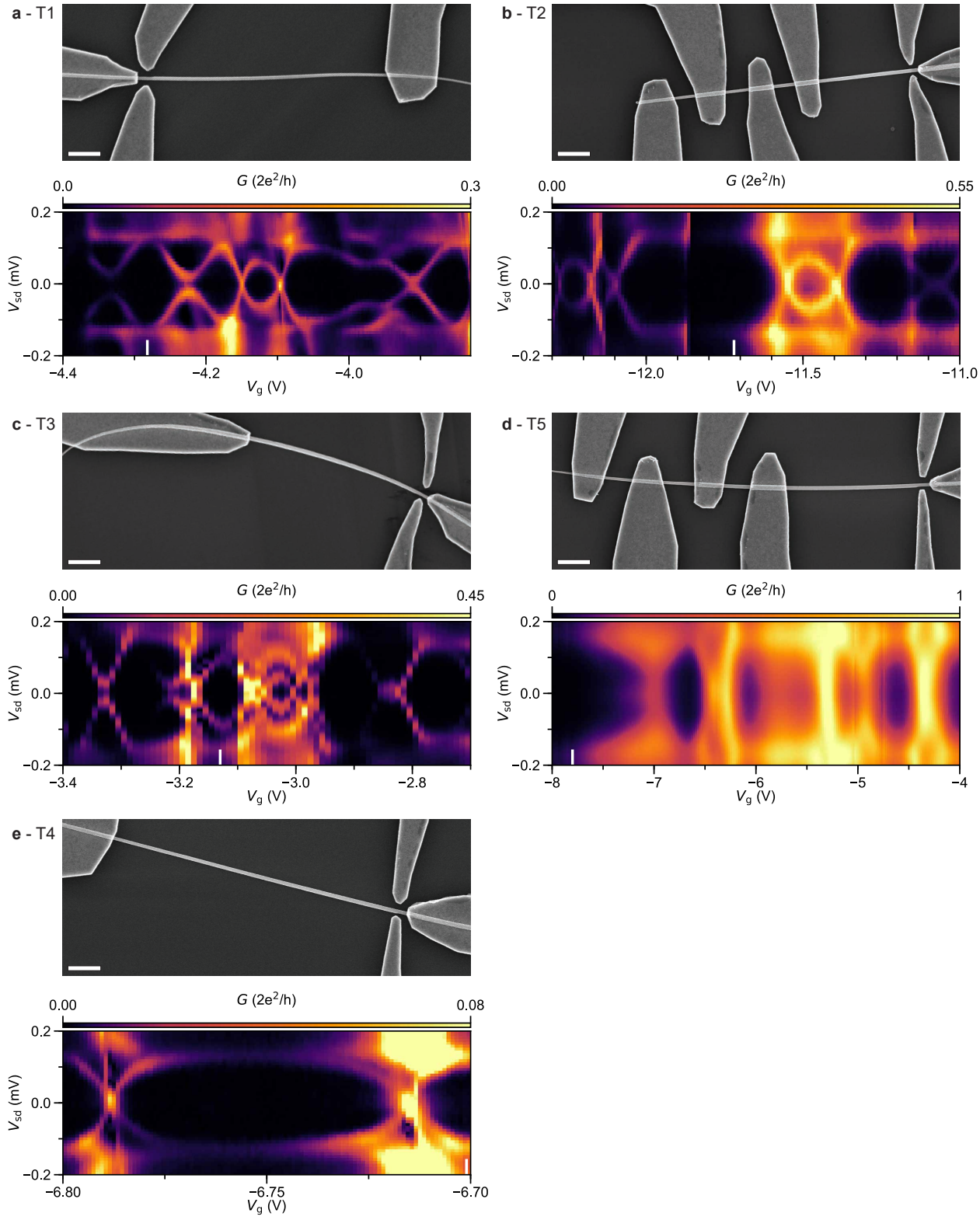

Figure S8. SEM and bias spectroscopy for devices in main text Fig. 3e (Ta coated, 20 nm thick). White lines in each spectroscopy panel show the V_g setting for line traces in main text Fig. 3d. Scale bars represent 1 μm.

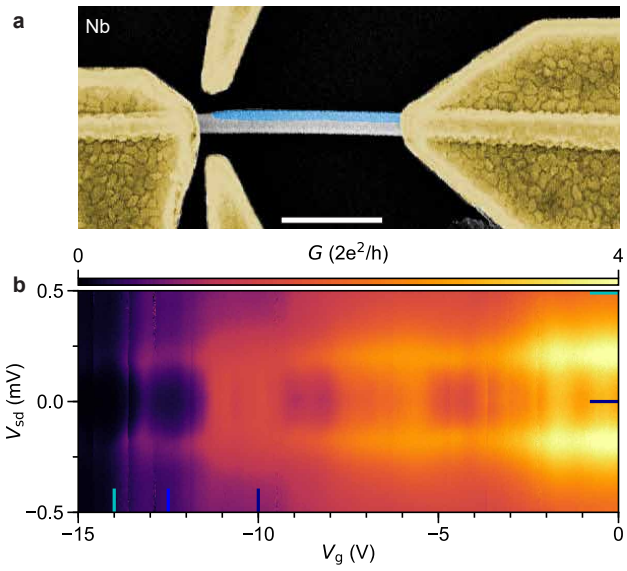

Figure S9. **a**, SEM of Nb coated (blue) device and **b**, bias spectroscopy from which the data in Figs 3f/g of the main text was extracted. The $V_{\rm sd}/V_{\rm g}$ settings for each line trace in main text Figs 3f/g are indicated by the coloured lines. Scale bar in **a** represents 500 nm.

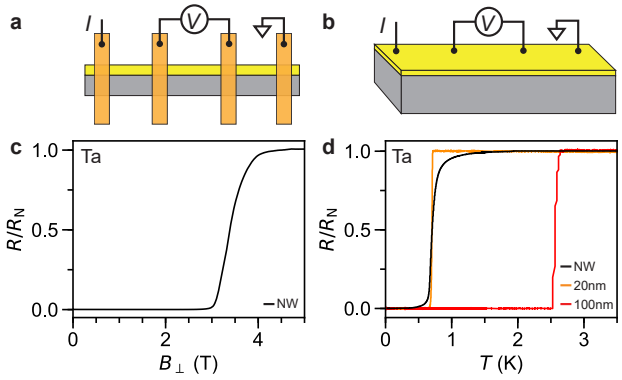

Figure S10. Four point resistance measurements on Ta thin films deposited on **a**, nanowires or **b**, bulk substrates. The 20 nm thick nanowire thin film exhibits **c**, perpendicular critical field $B_{\rm C} \sim 3.5$ T and **d**, critical temperature $T_{\rm C} \sim 0.7$ K. The 20 nm and 100 nm thick thin films had $T_{\rm C} \sim 0.7$ and 2.5 K, respectively.

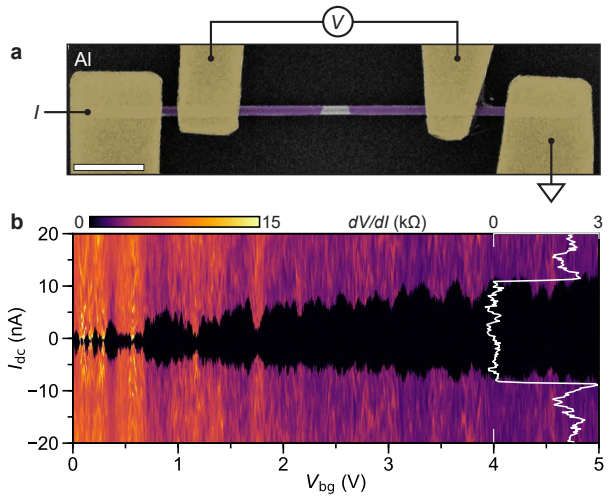

Figure S11. Gate-tunable Josephson junctions a, False-colour SEM of Al-coated (purple) SNS nanowire (grey), with constant dc current I sourced from one of four Ti/Au contacts (gold), and voltage V measured in a four-point configuration. The conducting substrate served as a back-gate. Scale bar represents 1 μm. **b**, Differential resistance dV/dI vs dc current $I_{\rm dc}$ and back-gate voltage $V_{\rm bg}$ shows the device has zero resistance for small $I_{\rm dc}$ less than critical current $I_{\rm C}$, modulated by $V_{\rm bg}$[16].

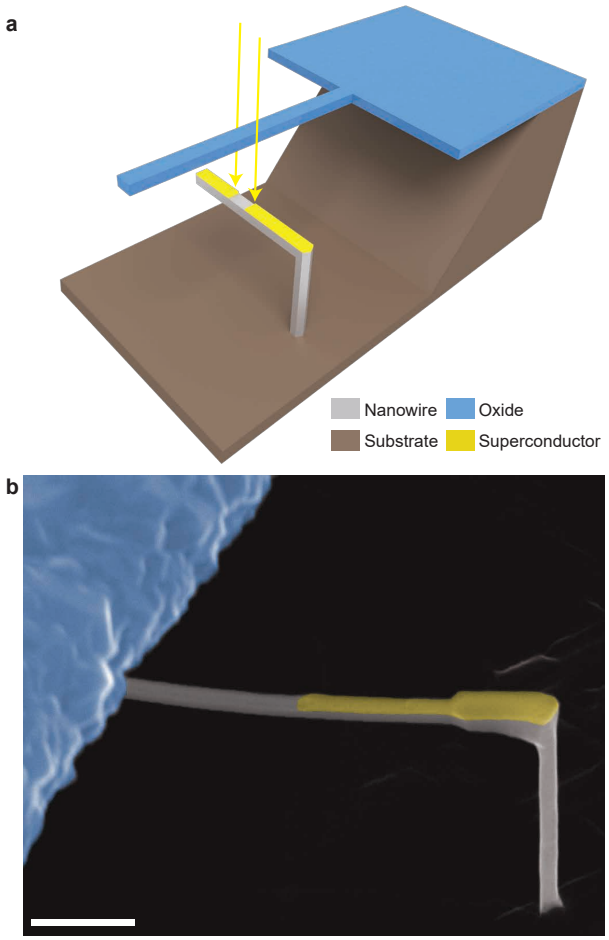

Figure S12. Application of the shadow platform to kinked nanowires. Superconductor (vanadium) is deposited from a direction perpendicular to the growth substrate. Scale bar represents 500 nm.

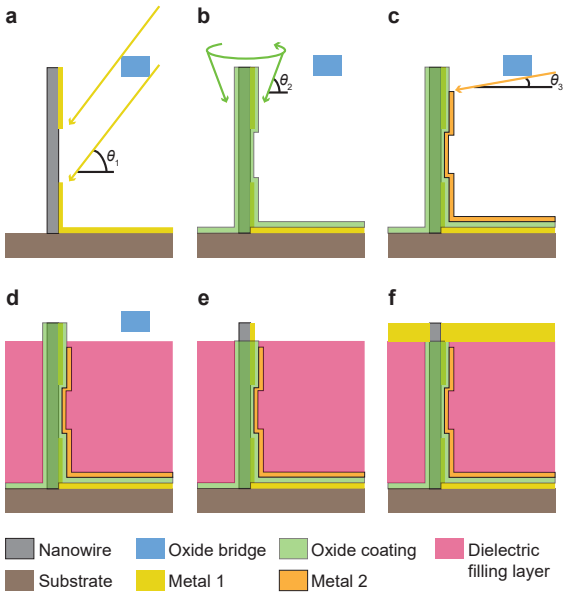

Figure S13. Suggested process flow for large scale nanowire device arrays, utilising the shadow mask platform; see text for detailed description.